Høgskolen i Østfold

EKSAMEN

Emnekode: **IRE 11518**	**Emnenavn:** **Digitalteknikk**
Dato: 11. juni 2019 **Sensurfrist: 2.juli 2019**	**Eksamenstid: 9:00 13:00**
Antall oppgavesider: 7 **Antall vedleggsider: 55**	**Faglærer: Reidar Nordby** **Oppgaven er kontrollert: Ja**

Hjelpemidler:
Floyd, T. L., Digital Fundamentals: A Systems Approach, Prentice Hall, 2013,
Kompendium HiØ / Åge T Johansen: Tallsystemer og koder
Kompendium HiØ /Åge T Johansen: Boolsk algebra og logiske funksjoner
Kompendium HiØ / Åge T Johansen: VHDL - hurtigreferanse

Om eksamensoppgaven:

Oppgavens vekt er oppgitt for hver deloppgave.

Lykke til!

Kandidaten må selv kontrollere at oppgavesettet er fullstendig

Høgskolen i Østfold

Tema VHDL:

Oppgave1: 10%

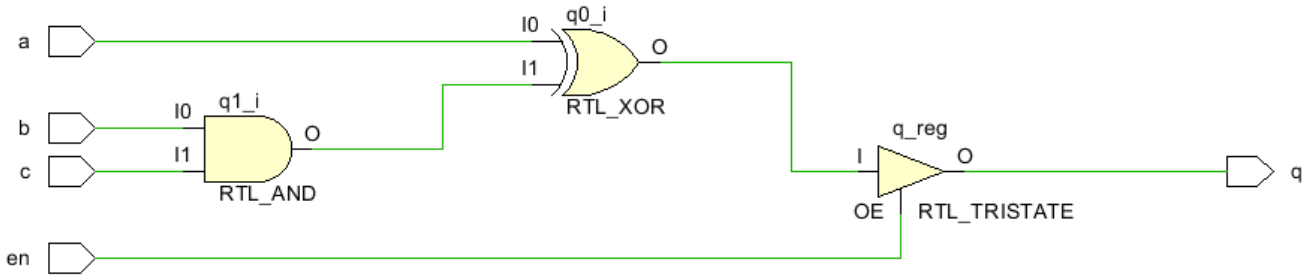
a) 2%
En VHDL-beskrivelse består i grunnversjonen av 2 hoved deler.
Hva heter hoveddelene?

b) 4%
Gi et eksempel på hva hoveddelene beskriver.

c) 4%
Hvordan brukes en VHDL testbenk (simulation source)?

Oppgave 2: 20%

Figur 1. viser en logisk funksjon:



Figur 1 Eksempel på et logisk uttrykk

a) 5%
Skriv sannhetstabellen til det logiske utrykket i figur 1.

b) 5%
Lag VHDL koden til inngangene og utgangen til Figur 1

c) 10%
Lag en VHDL kode som beskriver funksjonen i Figur 1.

Oppgave 3: 20%

FPGA-er fra Xilinx bruker at design verktøy som heter Vivado.

a) 10%
Nevn 4 sentrale funksjoner i Vivado.

b) 10%
I lab oppgave har det blitt brukt to forskjellige input filer til Vivado. VHDL filer og en constraints fil. Hva beskriver constraints filen?

Tema Tilstandsmaskiner; Trafikklys:

Oppgave 4 25%

Generelt :

Du skal konstruere styringen til et trafikklys med to kryssende gater.

Prinsippene er:
- skal konstrueres som en tilstandsmaskin
- klokke er generert eksternt og har en frekvens på 1 Hz.

Tilstandstabell:

tilstand	Nord Sør	Øst Vest
0	Rødt	Grønt
1	Rødt	Gult
2	Rødt	Rødt
3	Rødt og Gult	Rødt
4	Grønt	Rødt
5	Gult	Rødt
6	Rødt	Rødt
7	Rødt	Rødt og Gult

Det finnes følgende signaler ut av tilstandsmaskinen:

Navn Utgang	Funksjon på utgang
NRød	Rødt lys Nord-Sør
NGul	Gult lys Nord-Sør
NGrønn	Grønt lys Nord-Sør
VRød	Rødt lys Øst-Vest
VGul	Gult lys Øst-Vest
VGrønn	Grønt lys Øst-Vest

a) 2%
Tegn et generelt blokkskjema over en Moore maskin.

b) 4%
Tegn et blokkskjema av en Moore Maskin som styring for dette lyskrysset med inn og utganger som angitt.

c) 6%
Tegn tilstandsdiagram for tilstandsmaskinen, Moore maskin.

d)4%
Du skal benytte en synkron teller som kjerne i konstruksjonen. Telleren benytter T-flip- flopp'er benevnt A,B og C som minneelementer.
Sett opp nestetilstandstabell for telleren i lyskrysset[...0-7-0...]

e) 4%
Benytt Karnaugh diagram for å finne ligningene for T_A, T_B, og T_C og tegn logisk skjema for telleren i punktet over.

f) 5%
Benytt karnaugh diagram for å finne dekodingen av tellerens utganger til de seks utgangene NRød, NGul , HGrønn, VRød, VGul og VGrønn. Tegn logisk skjema.

Oppgave 5: 25%

Lyskrysset skal utstyres med følere i Nord - Sør retning for å prioritere trafikken Øst -Vest. Lyskrysset skal også ha brytere for gangfelt over kryssets Vestre og Nordere armer. Felles utganger for Rød og Grønn Person til fotgjengerfelt må derfor legges til. (i alt 2 stk.)
Konstruksjonen kan vesentlig forenkles ved å reorganisere tilstandstabellen, bruke en annen teller, en minnekrets som dekoder og innføre en latch på innsignalene.
Her skal vi også ta med tidsperspektivet.
Videre ønsker vi at sekvensene skal utføres komplett før ny sekvens starter. Vi legger derfor til en ekstra utgang "sekvens slutt" (SS)for dette formålet. Etter at sekvensen er ferdig skal vi alltid tilbake til «Normal» tilstanden (se under). «Normal»tilstanden skal alltid vare minst 30 sekunder.
Dersom bryter for fotgjenger og sensor for bil aktiveres samtidig skal fotgjengere slippes over først.

Reorganisert tilstandstabell:

Hoved tilstand	Innganger Fotgj,BilNS	Minne adresser	Nord Sør	Øst Vest	Fotgjenger	tid i sekunder
Normal	0,0	0-30	Rødt	Grønt	Rødt	30
innslipp N-S	0,1	0-4	Rødt	Gult	Rødt	5
		5-6	Rødt	Rødt	Rødt	2
		7-11	Rødt og Gult	Rødt	Rødt	5
		12-42	Grønt	Rødt	Rødt	30
		43-48	Gult	Rødt	Rødt	5
overslipp gangfelt	1,X	0-4	Rødt	Gult	Rødt	5
		5-6	Rødt	Rødt	Rødt	2
		7-11	Rødt	Rødt	Blinkende Grønt	6
		12-27	Rødt	Rødt	Grønt	15
		28-31	Rødt	Rødt	Blinkende Rødt	6

Oppgaveteksten fortsetter på neste side

Du har nå disse inngangene til tilstandsmaskinen:

Inngang	**Funksjon**
Klokke	1 Hz benyttes til trigging på POSITIV flanke.
Bil NS	Blir 1 når bil befinner seg i kryssende gate N-S
Fotgjenger	Fotgjenger har trykket inn bryter for kryssing.

Videre har du disse utgangene:

Navn Utgang	Funksjon på utgang
NRød	Rødt lys Nord-Sør
NGul	Gult lys Nord-Sør
NGrønn	Grønt lys Nord-Sør
VRød	Rødt lys Øst-Vest
VGul	Gult lys Øst-Vest
VGrønn	Grønt lys Øst-Vest
GFotgjenger	Grønn «Mann»
RFotgjenger	Rød «mann»
Sekvens_slutt	Blir «1» når sekvensen er ferdig

Gfotgjenger og Rfotgjenger skal blinke 3 ganger med en frekvens på 0,5 Hz før de blir faste. Gfotgenger skal deretter stå fast i 15 sekunder. Rfotgjenger står så lenge biltrafikk tillates.
Trafikk startes i Ø-V etter avbrudd av fotgjenger og innslipp fra Nord -Sør. Ø-V skal stå i minimum 30 sek.

Hint: La klokka og telleren gå hele tiden. «Sekvens slutt» benyttes til å resette telleren samt klokke for D-latcher

Du har til rådighet :

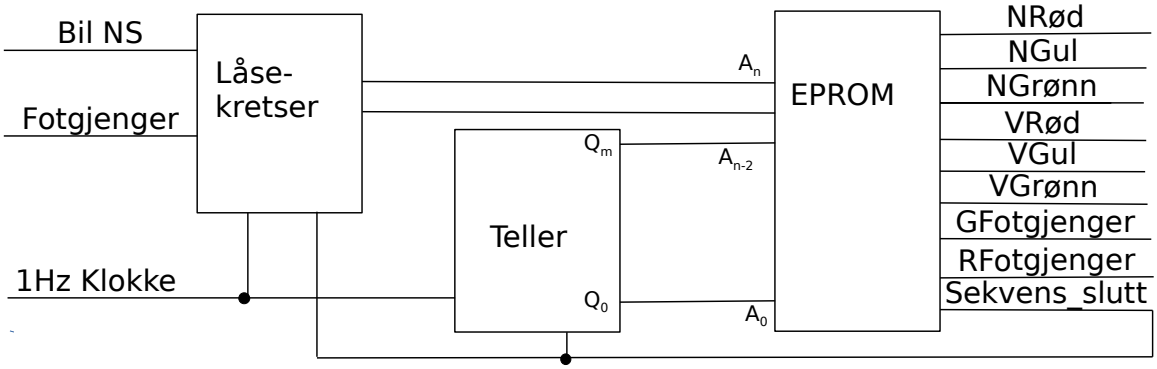
- Et antall EPROM minne 27W401 (datablad i vedlegg 3) de minste tilgjengelige i øyeblikket.

- Et antall 4 bits tellere type 74hc193 (datablad i vedlegg 2)

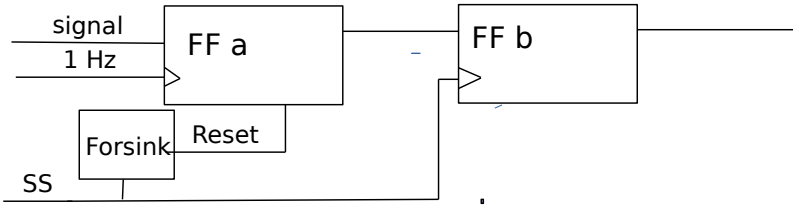
- Et antall 74hc74A; Dobbel D- flip-flop med klokking på stigende klokkeflanke og invertert resetinngang ($\overline{\text{Reset}}$). (Datablad er vist i vedlegg 1.)

Div. portkretser med logiske funksjoner.

Til støtte gis dette blokkskjemaet:



Låsekretsen låser til verdien på inngangen på stigende klokkeflanke, dette signalet overføres i sin tur til en latch som holder signalet stabilt gjennom hele sekvenser. Feks. når det er innslipp fra N-S.
Hint: benytt signalet "sekvens slutt" (SS) til å klokke utgangslatch, benytt samme signal , men forsinket til å resette inngangsvippa.



a) 10%
Konstruer (tegn logisk skjema av) låsekretsblokka ved hjelp av D-vippene og nødvendige logiske porter. Det kan hende du må forsinke enkelte signaler, - benytt i tilfelle invertere i serie. Tegn vei - tid skjema for blokka.

b) 2.5%
Hvor lang er en sekvens med avbrudd fra N-S i sekunder? Hvor mange klokkeperioder er dette?

c) 2,5%
Hvor mange adresseinnganger har minnekretsen 27W401?
Hvor mange adresseinnganger trenger du?
Hva blir det aktuelle navnet på inngangen merket A_n på EPROM'en i figuren over?

d) 7,5%
Benytt dine kunnskaper og hint foran for å tegne et fullstendig logisk skjema for kretsen. Ta utgangspunkt i de foreslåtte komponentene. Det skal tydelig framgå hvordan du kobler telleren og EPROM'ene.

e) 2,5%
Lag en tabell som angir innholdet i adressene i Eprom’ene! Ta utgangspunkt i tabellen på side 5.

SLUTT PÅ OPPGAVETEKST

VEDLEGG 1

MC74HC74A

Dual D Flip-Flop with Set and Reset

High–Performance Silicon–Gate CMOS

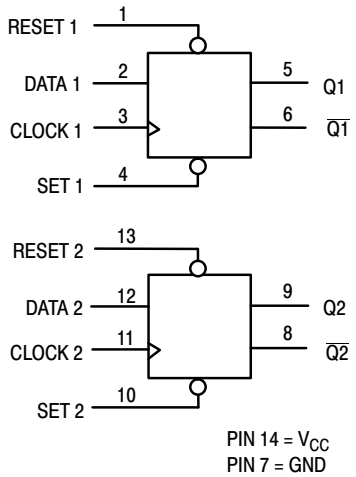
The MC74HC74A is identical in pinout to the LS74. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of two D flip–flops with individual Set, Reset, and Clock inputs. Information at a D–input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and $\overline{Q}$ outputs are available from each flip–flop. The Set and Reset inputs are asynchronous.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 128 FETs or 32 Equivalent Gates
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

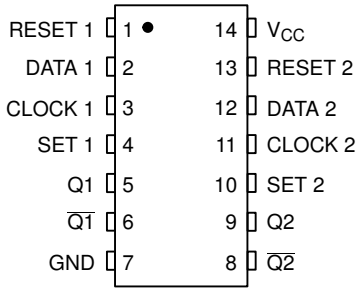
ON Semiconductor®

http://onsemi.com

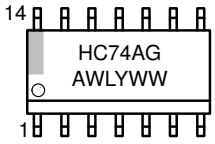
SOIC–14 NB
D SUFFIX
CASE 751A

TSSOP–14
DT SUFFIX
CASE 948G

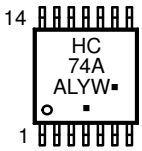
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC–14 NB



TSSOP–14

A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

FUNCTION TABLE

Inputs				Outputs	
Set	**Reset**	**Clock**	**Data**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	No Change	
H	H	H	X	No Change	
H	H	↓	X	No Change	

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, SOIC Package†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(SOIC or TSSOP Package)	260	
		300	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: –7 mW/°C from 65° to 125°C
TSSOP Package: –6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		–55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
	(Figures 1, 2, 3)	V_{CC} = 3.0 V	0	600	
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\| \le 20$ μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 4.0$ mA $\|I_{out}\| \le 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	2.0	20	80	μA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figures 1 and 4)	2.0 3.0 4.5 6.0	100 75 20 17	125 90 25 21	150 120 30 26	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Set or Reset to Q or $\overline{Q}$ (Figures 2 and 4)	2.0 3.0 4.5 6.0	105 80 21 18	130 95 26 22	160 130 32 27	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Flip–Flop)*	32	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	2.0 3.0 4.5 6.0	80 35 16 14	100 45 20 17	120 55 24 20	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	2.0 3.0 4.5 6.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	3.0 3.0 3.0 3.0	ns
t_{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock (Figure 2)	2.0 3.0 4.5 6.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	8.0 8.0 8.0 8.0	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	2.0 3.0 4.5 6.0	60 25 12 10	75 30 15 13	90 40 18 15	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figures 1, 2, 3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

ORDERING INFORMATION

Device	Package	Shipping†
MC74HC74ADG	SOIC–14 NB (Pb–Free)	55 Units / Rail
NLV74HC74ADG*	SOIC–14 NB (Pb–Free)	55 Units / Rail
MC74HC74ADR2G	SOIC–14 NB (Pb–Free)	2500 / Tape & Reel
NLV74HC74ADR2G*	SOIC–14 NB (Pb–Free)	2500 / Tape & Reel
MC74HC74ADTR2G	TSSOP–14 (Pb–Free)	2500 / Tape & Reel
NLV74HC74ADTR2G*	TSSOP–14 (Pb–Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

SWITCHING WAVEFORMS

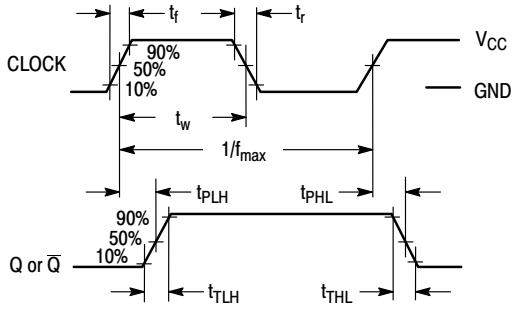


Figure 1.

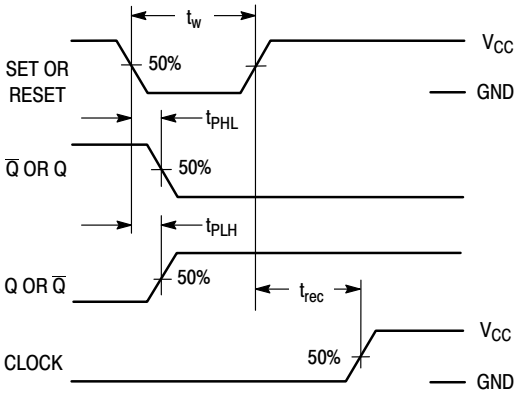


Figure 2.

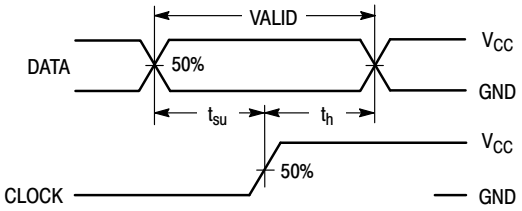


Figure 3.

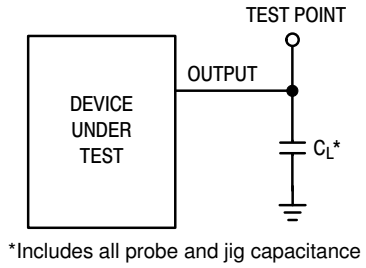


Figure 4.

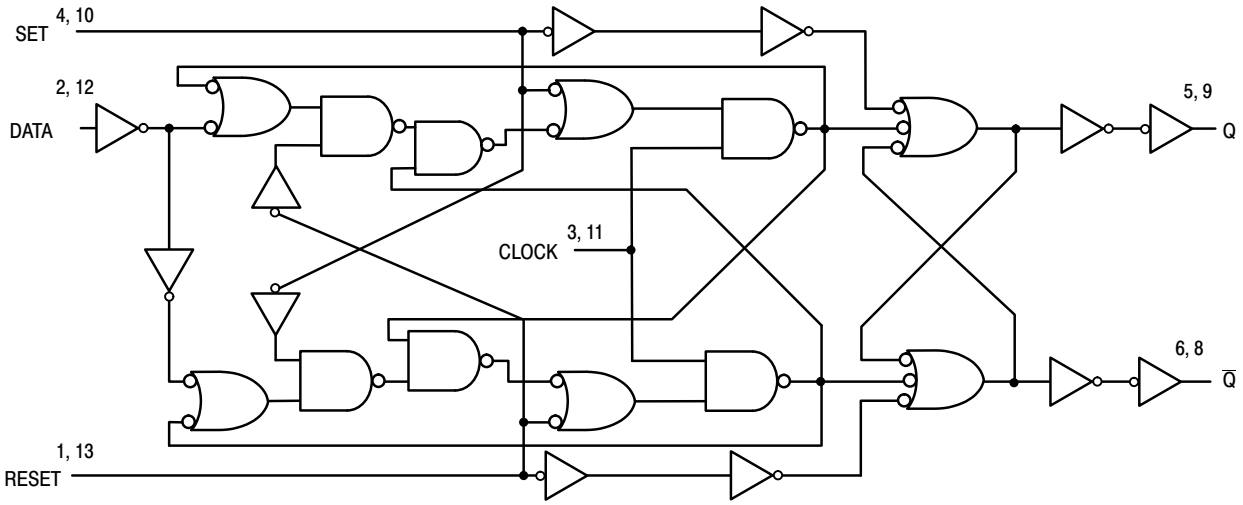
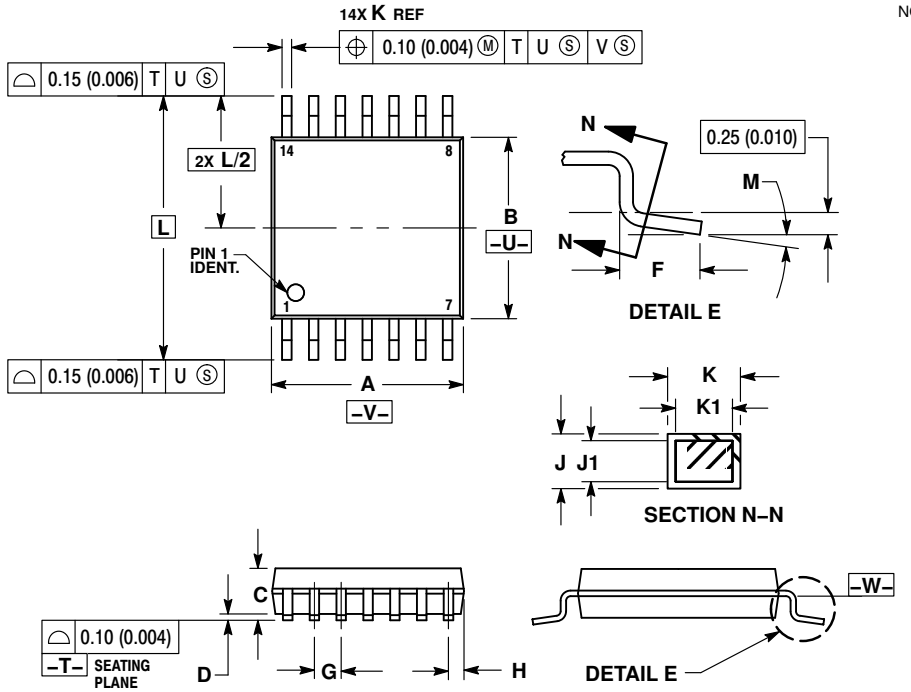


Figure 5. EXPANDED LOGIC DIAGRAM

PACKAGE DIMENSIONS

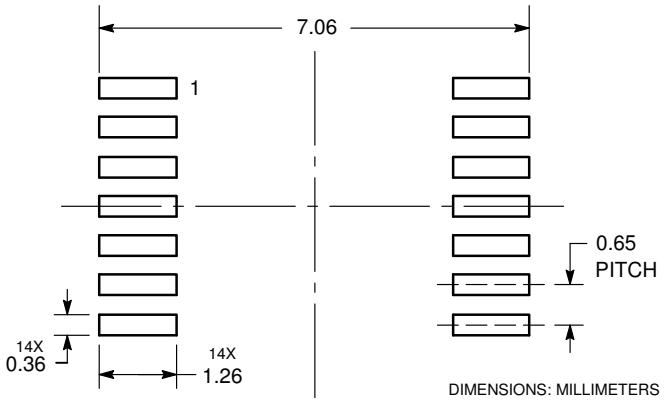
TSSOP–14
CASE 948G
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

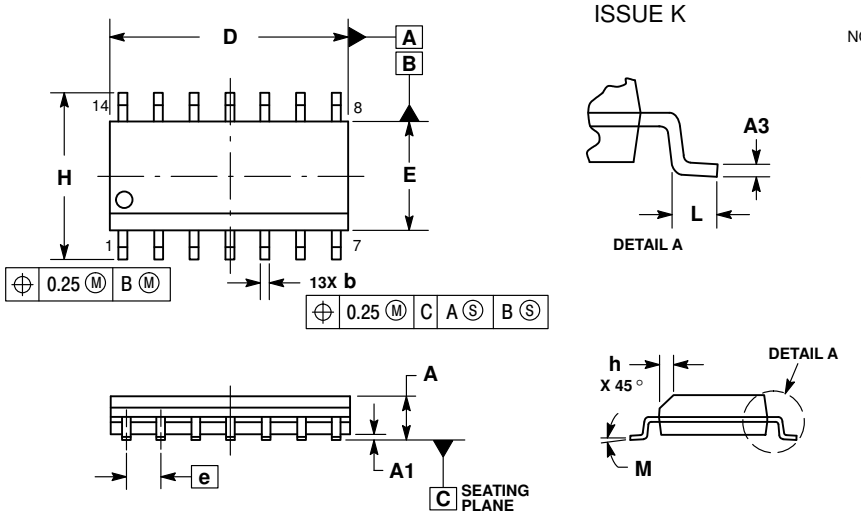
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

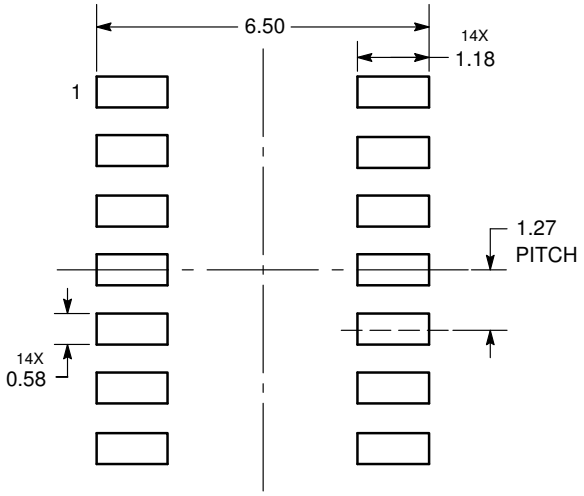
SOIC–14 NB
CASE 751A–03
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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VEDLEGG 2

CD54/74HC192, CD54/74HC193, CD54/74HCT193

Data sheet acquired from Harris Semiconductor
SCHS163F

September 1997 - Revised October 2003

High-Speed CMOS Logic Presettable Synchronous 4-Bit Up/Down Counters

Features

- **Synchronous Counting and Asynchronous Loading**
- **Two Outputs for N-Bit Cascading**
- **Look-Ahead Carry for High-Speed Counting**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55^{o}C to 125^{o}C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, V_{IL}= 0.8V (Max), V_{IH} = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}**

Description

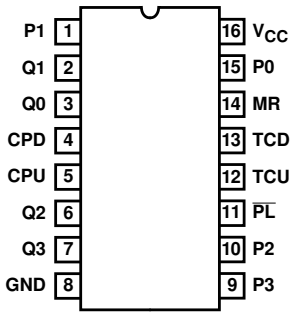
The ’HC192, ’HC193 and ’HCT193 are asynchronously presettable BCD Decade and Binary Up/Down synchronous counters, respectively.

Presetting the counter to the number on the preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ($\overline{PL}$). The counter is incremented on the low-to-high transition of the Clock-Up input (and a high level on the Clock-Down input) and decremented on the low to high transition of the Clock-Down input (and a high level on the Clock-up input). A high level on the MR input overrides any other input to clear the counter to its zero state. The Terminal Count up (carry) goes low half a clock period before the zero count is reached and returns to a high level at the zero count. The Terminal Count Down (borrow) in the count down mode likewise goes low half a clock period before the maximum count (9 in the 192 and 15 in the 193) and returns to high at the maximum count. Cascading is effected by connecting the carry and borrow outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

Pinout

CD54HC192, CD54HC193, CD54HCT193 (CERDIP)
CD74HC192 (PDIP, SOP, TSSOP)
CD74HC193 (PDIP, SOIC)
CD74HCT193 (PDIP)
TOP VIEW



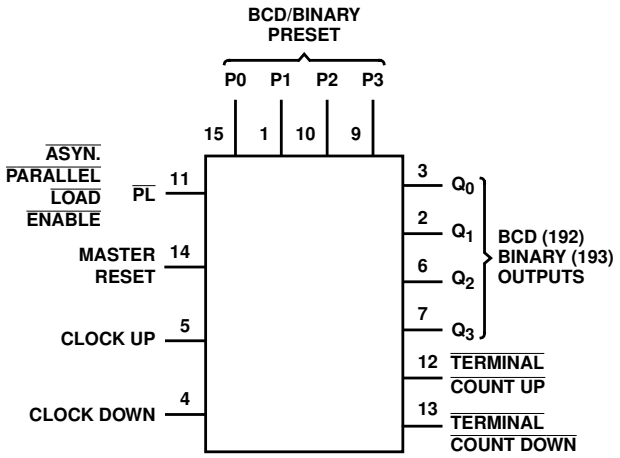
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
CD54HC192F3A	-55 to 125	16 Ld CERDIP
CD54HC193F3A	-55 to 125	16 Ld CERDIP
CD54HCT193F3A	-55 to 125	16 Ld CERDIP
CD74HC192E	-55 to 125	16 Ld PDIP
CD74HC192NSR	-55 to 125	16 Ld SOP
CD74HC192PW	-55 to 125	16 Ld TSSOP
CD74HC192PWR	-55 to 125	16 Ld TSSOP
CD74HC192PWT	-55 to 125	16 Ld TSSOP
CD74HC193E	-55 to 125	16 Ld PDIP
CD74HC193M	-55 to 125	16 Ld SOIC
CD74HC193MT	-55 to 125	16 Ld SOIC
CD74HC193M96	-55 to 125	16 Ld SOIC
CD74HCT193E	-55 to 125	16 Ld PDIP

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Diagram



TRUTH TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FUNCTION
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset Inputs

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} or I_{GND} . . . . . ±50mA

Operating Conditions

Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
E (PDIP) Package . . . . . 67°C/W
M (SOIC) Package. . . . . 73°C/W
NS (SOP) Package . . . . . 64°C/W
PW (TSSOP) Package . . . . . 108°C/W
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	µA

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS			25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT TYPES												
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	-	5.5	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 2)	V_{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	µA

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
P0-P3	0.4
MR	1.45
$\overline{PL}$	0.85
CPU, CPD	1.45

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g. 360µA max at 25°C.

Prerequisite For Switching Specifications

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
Pulse Width	t_W	2	115	-	-	145	-	175	-	ns
CPU, CPD		4.5	23	-	-	29	-	35	-	ns
192		6	20	-	-	25	-	30	-	ns
	t_W	2	100	-	-	125	-	150	-	ns
CPU, CPD		4.5	20	-	-	25	-	30	-	ns
193		6	17	-	-	21	-	26	-	ns
$\overline{PL}$	t_W	2	80	-	-	100	-	120	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR	t_W	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
Set-up Time	t_{SU}	2	80	-	-	100	-	120	-	ns
Pn to $\overline{PL}$		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
Hold Time	t_H	2	0	-	-	0	-	0	-	ns
Pn to $\overline{PL}$		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
Hold Time	t_H	2	80	-	-	100	-	120	-	ns
CPD to CPU or		4.5	16	-	-	20	-	24	-	ns
CPU to CPD		6	14	-	-	17	-	20	-	ns
Recovery Time	t_{REC}	2	80	-	-	100	-	120	-	ns
$\overline{PL}$ to CPU, CPD		4.5	16	-	-	20	-	24	-	ns
		6	14	-	-	17	-	20	-	ns
MR to CPU, CPD	t_{REC}	2	5	-	-	5	-	5	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	5	-	-	5	-	5	-	ns
Maximum Frequency	f_{MAX}	2	5	-	-	4	-	3	-	MHz
CPU, CPD		4.5	22	-	-	18	-	15	-	MHz
192		6	24	-	-	21	-	18	-	MHz
	f_{MAX}	2	5	-	-	4	-	3	-	MHz
CPU, CPD		4.5	25	-	-	20	-	17	-	MHz
193		6	29	-	-	24	-	20	-	MHz
HCT TYPES										
Pulse Width	t_W	2	-	-	-	-	-	-	-	ns
CPU, CPD		4.5	23	-	-	29	-	35	-	ns
192		6	-	-	-	-	-	-	-	ns
CPU, CPD	t_W	2	-	-	-	-	-	-	-	ns
193		4.5	23	-	-	29	-	35	-	ns
		6	-	-	-	-	-	-	-	ns

Prerequisite For Switching Specifications **(Continued)**

PARAMETER	SYMBOL	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{PL}$	t_W	2	-	-	-	-	-	-	-	ns
		4.5	16	-	-	20	-	24	-	ns
		6	-	-	-	-	-	-	-	ns
MR	t_W	2	-	-	-	-	-	-	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	-	-	-	-	-	-	-	ns
Set-up Time	t_{SU}	2	-	-	-	-	-	-	-	ns
Pn to $\overline{PL}$		4.5	15	-	-	19	-	22	-	ns
		6	-	-	-	-	-	-	-	ns
Hold Time	t_H	2	-	-	-	-	-	-	-	ns
Pn to $\overline{PL}$		4.5	0	-	-	0	-	0	-	ns
		6	-	-	-	-	-	-	-	ns
Hold Time	t_H	2	-	-	-	-	-	-	-	ns
CPD to CPU or		4.5	16	-	-	20	-	24	-	ns
CPU to CPD		6	-	-	-	-	-	-	-	ns
Recovery Time	t_{REC}	2	-	-	-	-	-	-	-	ns
$\overline{PL}$ to CPU, CPD		4.5	15	-	-	19	-	22	-	ns
		6	-	-	-	-	-	-	-	ns
MR to CPU, CPD	t_{REC}	2	-	-	-	-	-	-	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	-	-	-	-	-	-	-	ns
Maximum Frequency	f_{MAX}	2	-	-	-	-	-	-	-	MHz
CPU, CPD		4.5	22	-	-	18	-	15	-	MHz
192		6	-	-	-	-	-	-	-	MHz
CPU, CPD	f_{MAX}	2	-	-	-	-	-	-	-	MHz
193		4.5	22	-	-	18	-	15	-	MHz
		6	-	-	-	-	-	-	-	MHz

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	125	-	155	-	190	ns
CPU to $\overline{TCU}$		C_L = 50pF	4.5	-	-	25	-	31	-	38	ns
		C_L = 15pF	5	-	10	-	-	-	-	-	ns
		C_L = 50pF	6	-		21	-	26	-	32	ns
CPD to $\overline{TCD}$	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	125	-	155	-	190	ns
		C_L = 50pF	4.5	-	-	25	-	31	-	38	ns
		C_L = 15pF	5	-	10	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	21	-	26	-	32	ns
CPU to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	220	-	270	-	325	ns
		C_L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	37	-	46	-	55	ns

Switching Specifications Input t_r, t_f = 6ns **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
CPD to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	220	-	270	-	325	ns
		C_L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C_L = 15pF	5	-	18	-	-	-	-		ns
		C_L = 50pF	6	-	-	37	-	46	-	55	ns
$\overline{PL}$ to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	220	-	275	-	330	ns
		C_L = 50pF	4.5	-	-	44	-	55	-	66	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	37	-	47	-	56	ns
MR to Q_n	t_{PHL}	C_L = 50pF	2	-	-	200	-	250	-	300	ns
		C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	5	-	17	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	34	-	43	-	51	ns
Transition Time Q, TCU, TCD	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L = 15pF	5	-	40	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay CPU to $\overline{TCU}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	27	-	34	-	41	ns
		C_L = 15pF	5	-	11	-	-	-	-	-	ns
CPU to $\overline{TCD}$	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	27	-	34	-	41	ns
		C_L = 15pF	5	-	11	-	-	-	-	-	ns
CPU to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	5	-	17	-	-	-	-	-	ns
CPD to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	40	-	50	-	60	ns
		C_L = 15pF	5	-	17	-	-	-	-	-	ns
$\overline{PL}$ to Q_n	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	46	-	58	-	69	ns
		C_L = 15pF	5	-	21	-	-	-	-	-	ns
MR to Q_n	t_{PHL}	C_L = 50pF	4.5	-	-	43	-	54	-	65	ns
		C_L = 15pF	5	-	18	-	-	-	-	-	ns
Transition Time Q, TCU, TCD	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_{IN}	C_L = 50pF	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 3, 4)	C_{PD}	C_L = 15pF	5	-	50	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per gate.
4. $P_D = V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

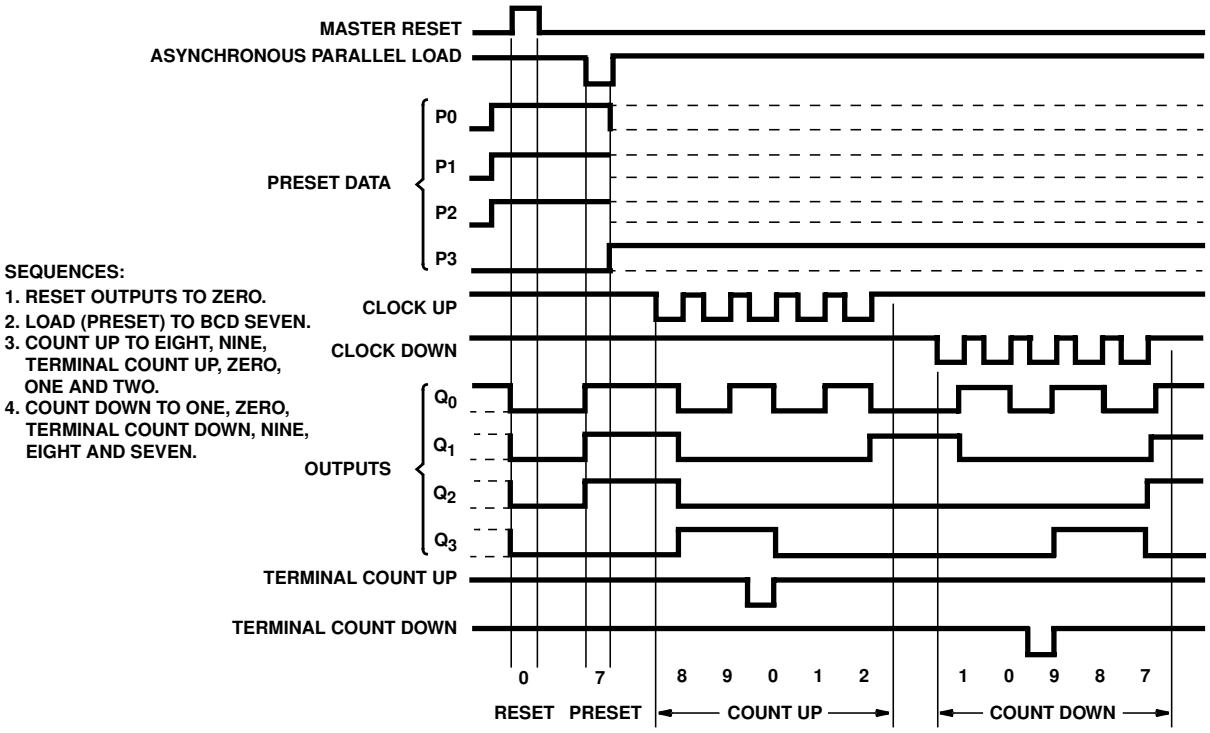
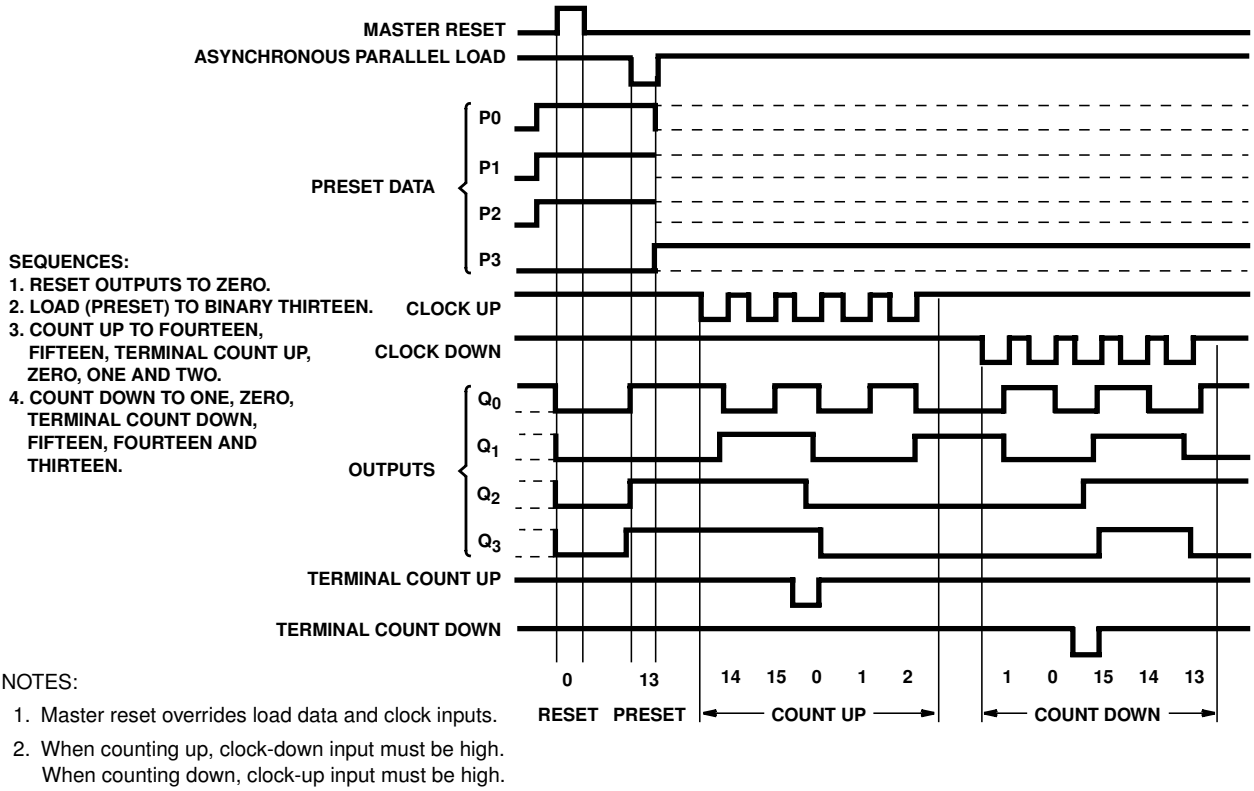


FIGURE 1. 'HC192 SYNCHRONOUS DECADE COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

Test Circuits and Waveforms (Continued)



NOTES:

1. Master reset overrides load data and clock inputs.
2. When counting up, clock-down input must be high. When counting down, clock-up input must be high.

FIGURE 2. 'HC193 SYNCHRONOUS BINARY COUNTERS, TYPICAL RESET, PRESET AND COUNT SEQUENCES

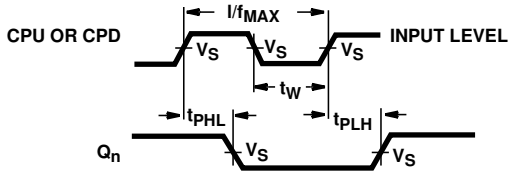


FIGURE 3. CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH

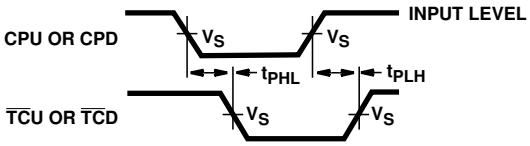


FIGURE 4. CLOCK TO TERMINAL COUNT DELAYS

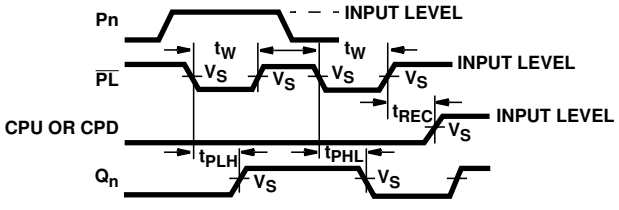


FIGURE 5. PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME

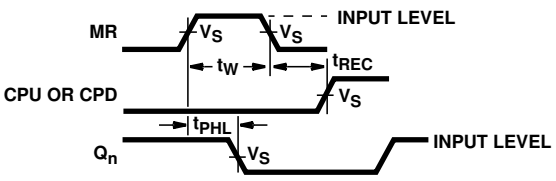


FIGURE 6. MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME

Test Circuits and Waveforms (Continued)

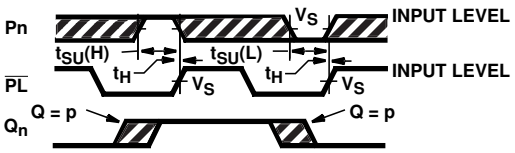


FIGURE 7. SET-UP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)

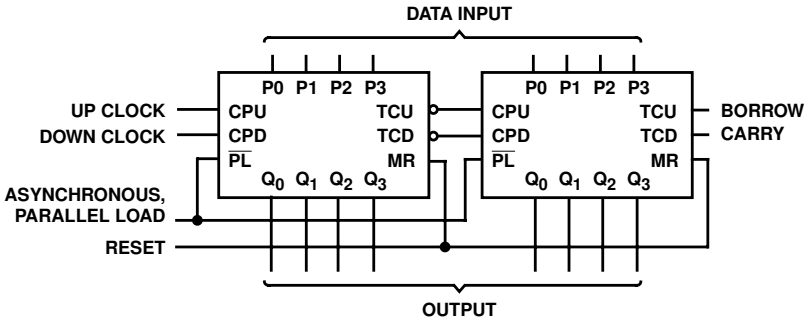
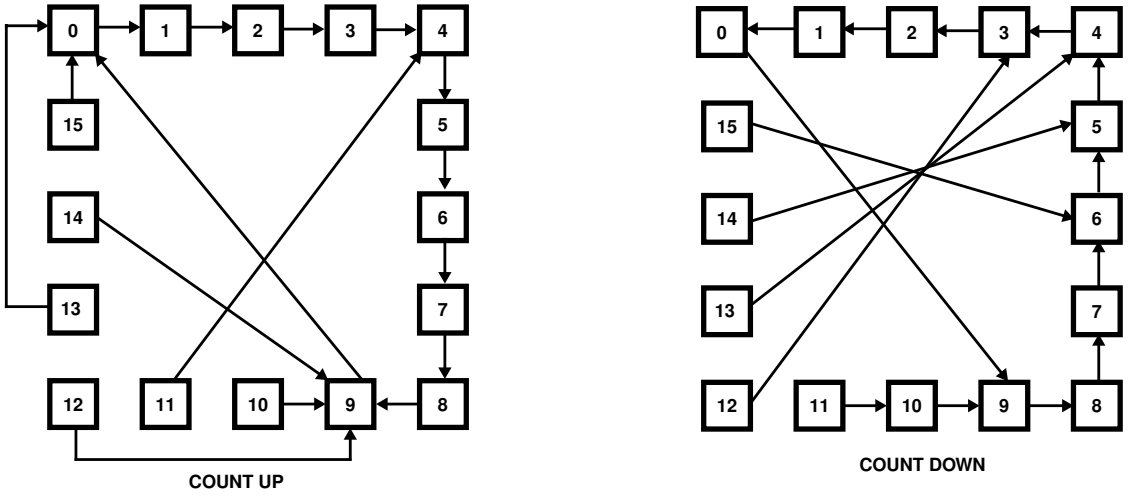


FIGURE 8. CASCADED UP/DOWN COUNTER WITH PARALLEL LOAD



NOTE: Illegal states in BCD counters corrected in one count.

NOTE: Illegal states in BCD counters corrected in one or two counts.

FIGURE 9. 'HC192, 'HCT193 STATE DIAGRAMS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8780801EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780801EA CD54HC192F3A	Samples
5962-9084801MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9084801MEA CD54HCT193F3A	Samples
CD54HC192F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8780801EA CD54HC192F3A	Samples
CD54HC193F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8772401EA CD54HC193F3A	Samples
CD54HCT193F3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9084801MEA CD54HCT193F3A	Samples
CD74HC192E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC192E	Samples
CD74HC192NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC192M	Samples
CD74HC192NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC192M	Samples
CD74HC192PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ192	Samples
CD74HC192PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ192	Samples
CD74HC192PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ192	Samples
CD74HC193E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC193E	Samples
CD74HC193M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC193M	Samples
CD74HC193M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC193M	Samples
CD74HC193M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC193M	Samples
CD74HC193MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC193M	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT193E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT193E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC192, CD54HC193, CD54HCT193, CD74HC192, CD74HC193, CD74HCT193 :

- Catalog: CD74HC192, CD74HC193, CD74HCT193

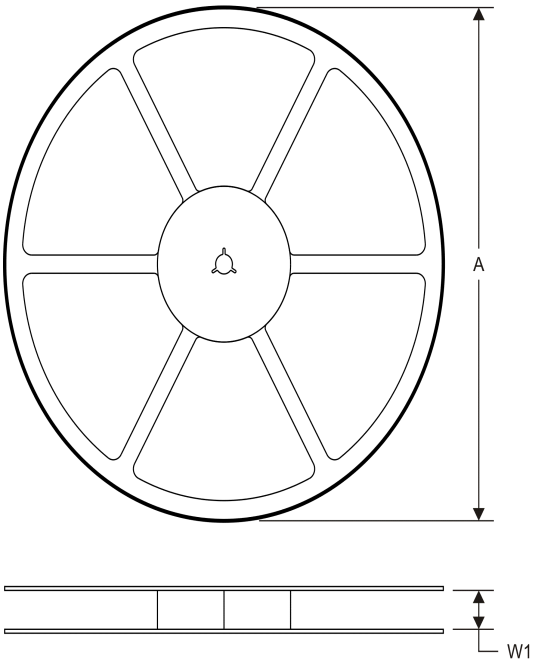
- Military: CD54HC192, CD54HC193, CD54HCT193

NOTE: Qualified Version Definitions:

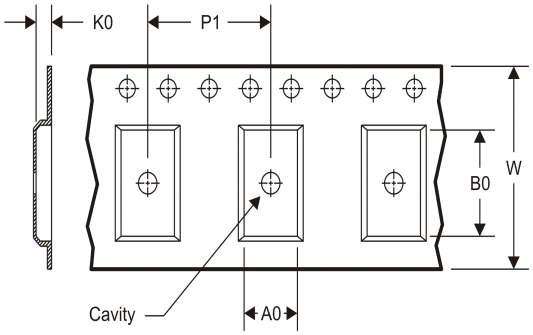
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



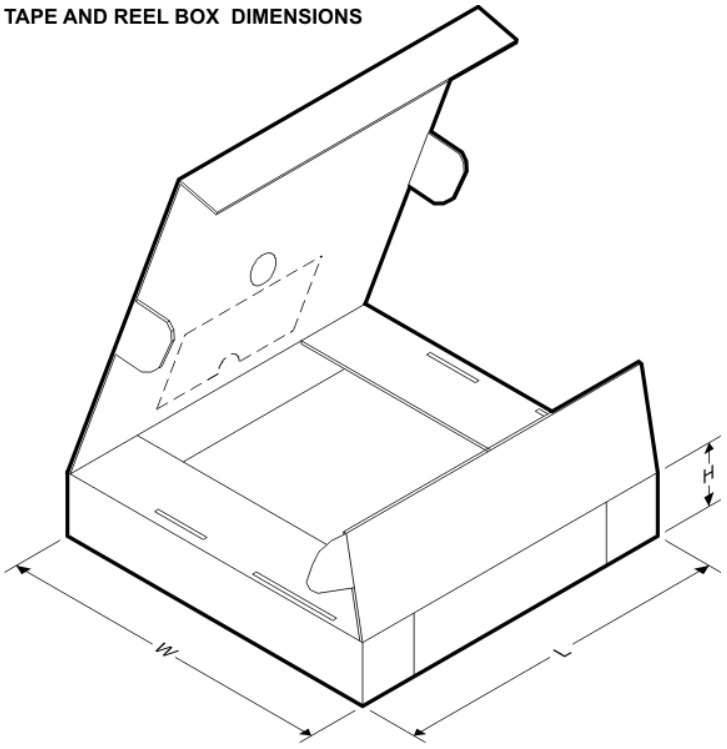
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC192NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD74HC192PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC192PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC193M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

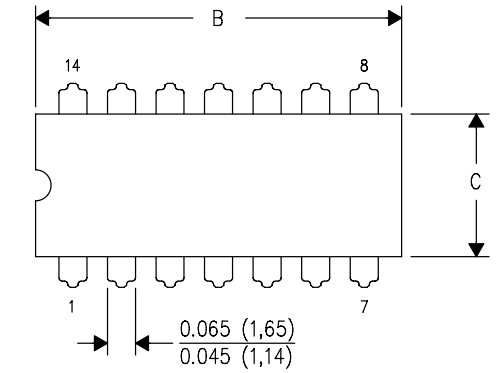


*All dimensions are nominal

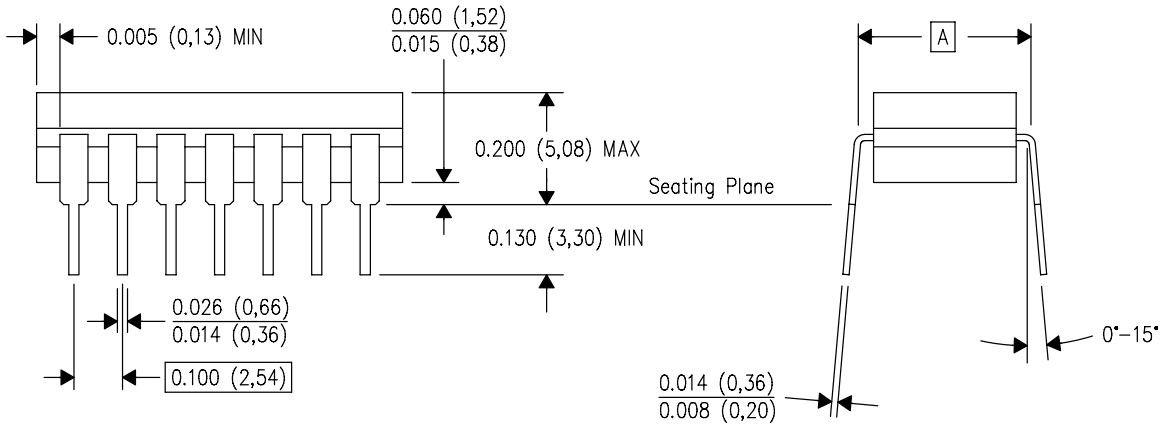
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC192NSR	SO	NS	16	2000	367.0	367.0	38.0
CD74HC192PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC192PWT	TSSOP	PW	16	250	367.0	367.0	35.0
CD74HC193M96	SOIC	D	16	2500	333.2	345.9	28.6

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



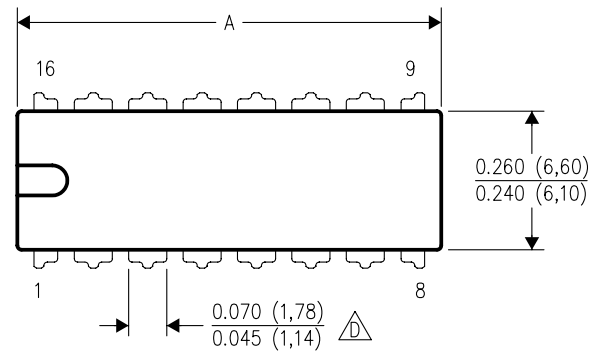
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

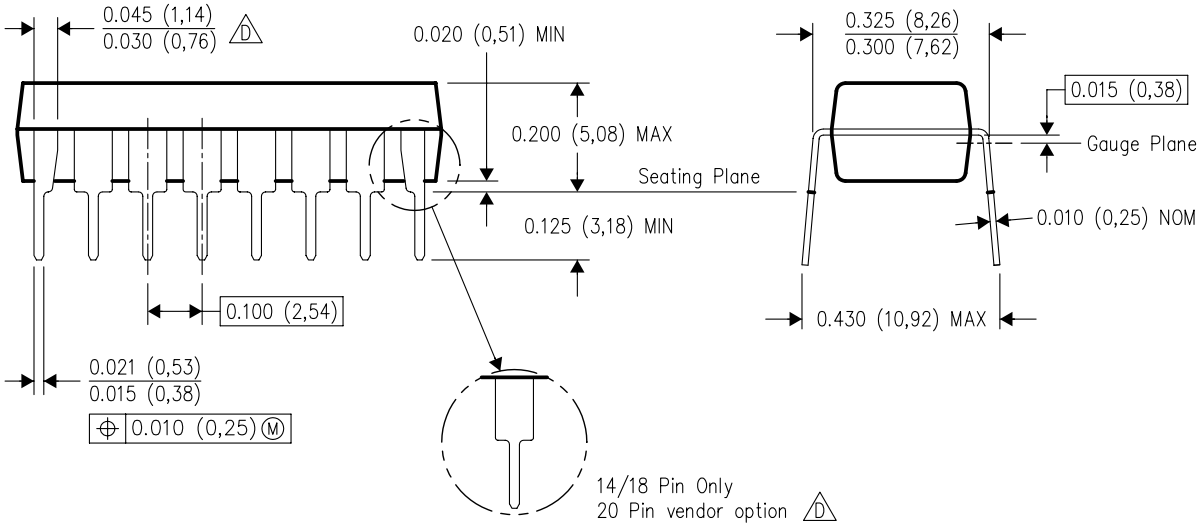
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



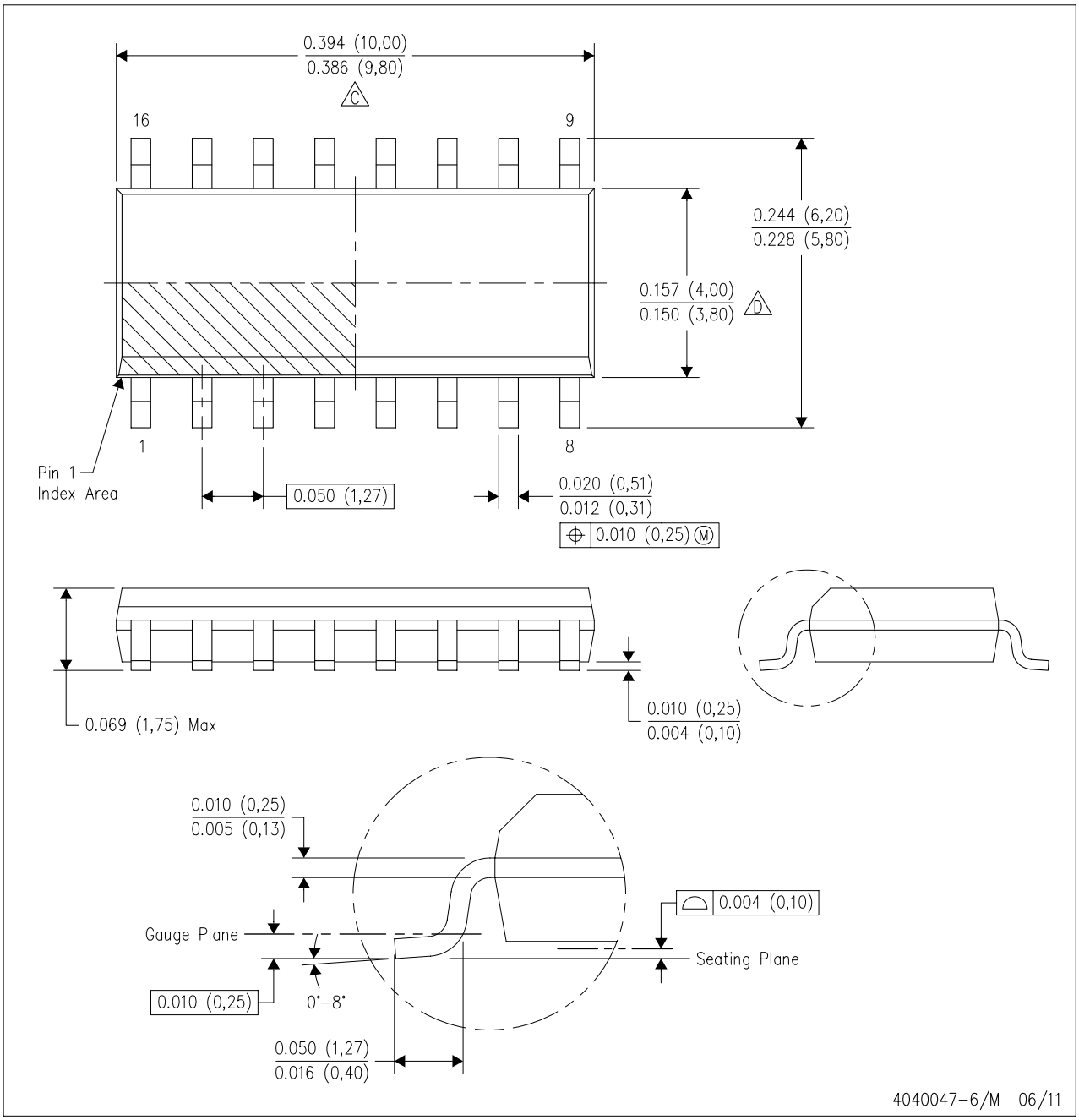
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

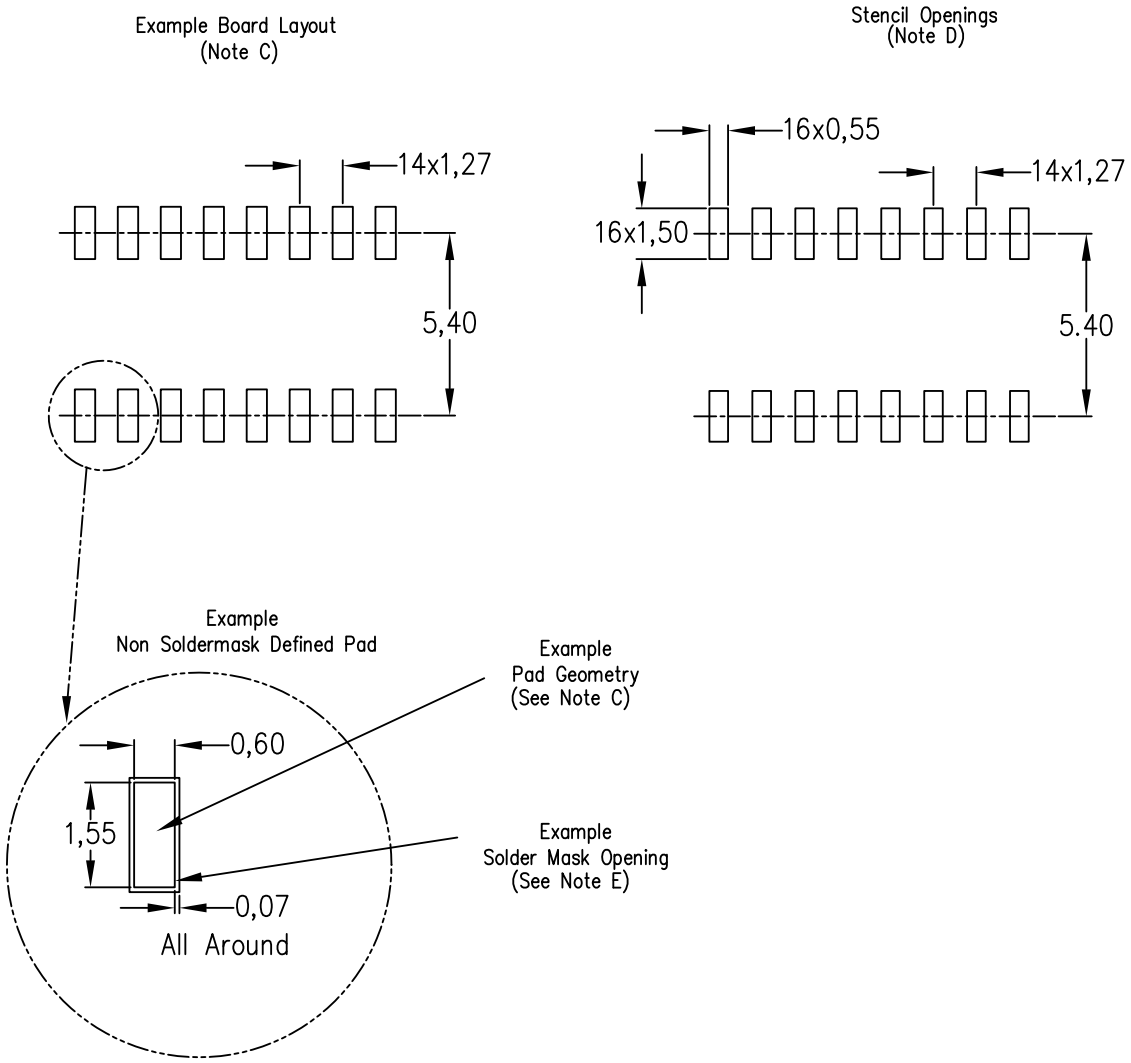
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



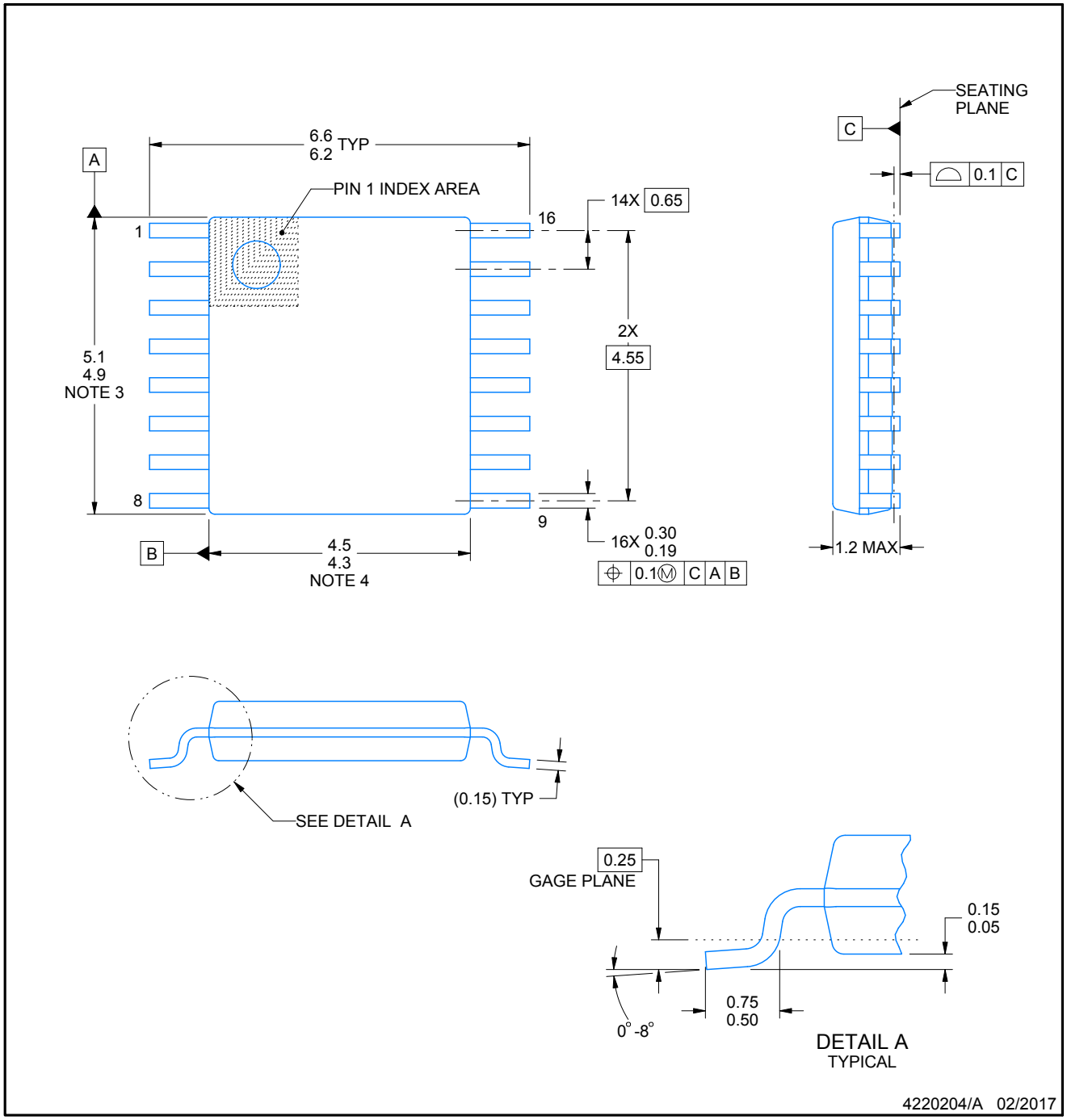
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

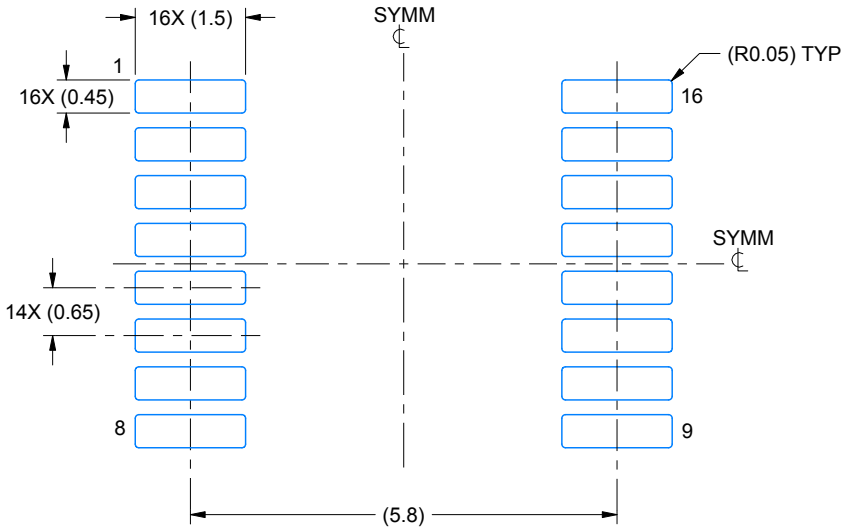
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

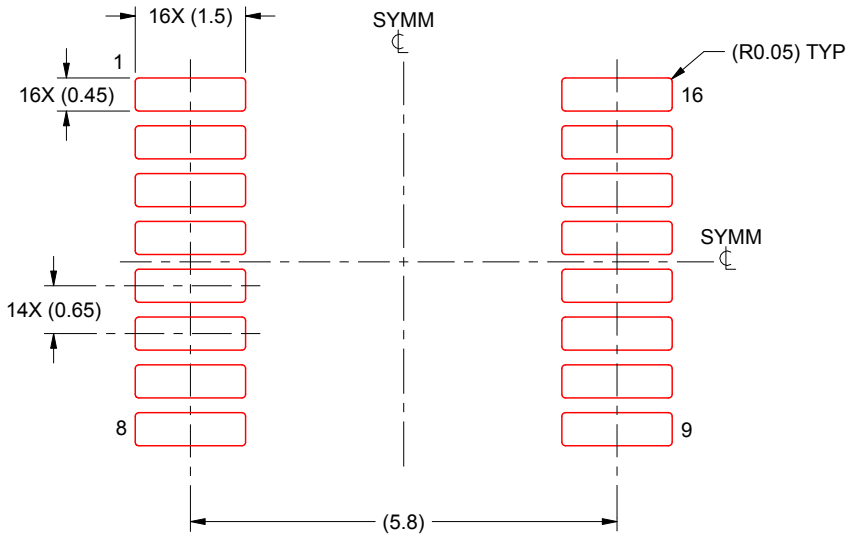
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

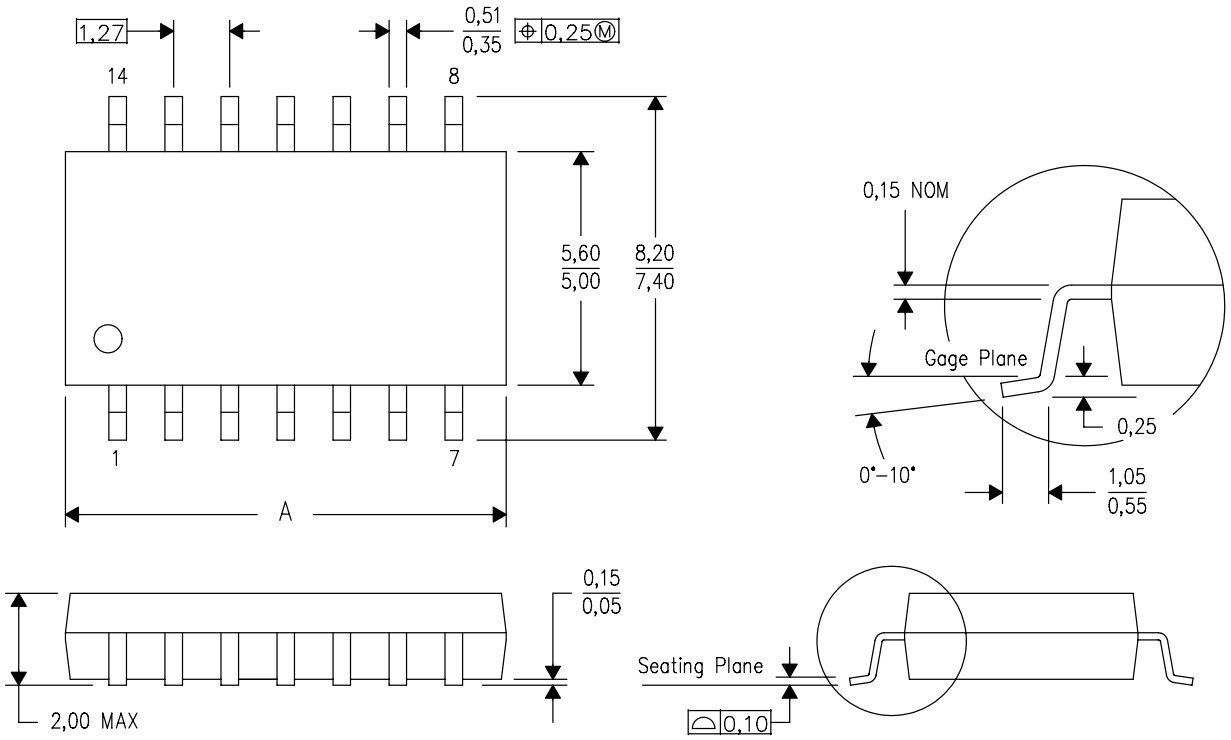
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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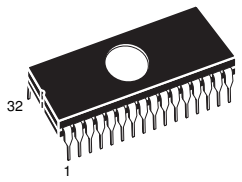
VEDLEGG 3

M27W401

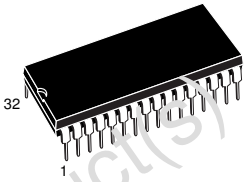
4 Mbit (512Kb x 8) Low Voltage UV EPROM and OTP EPROM

Features

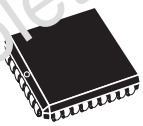
- 2.7V to 3.6V Supply Voltage in Read Operation
- Access Time:
  - 70 ns at V_{CC} = 3.0V to 3.6V
  - 80 ns at V_{CC} = 2.7V to 3.6V
- Pin Compatible with M27C4001
- Low Power Consumption:
  - 15 µA Max. Standby Current
  - 15 mA Max. Active Current at 5 MHz
- Programming Time 100 µs/byte
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Protection Immunity
- Electronic Signature
  - Manufacturer Code: 20h
  - Device Code: 41h
- ECOPACK® packages available



FDIP32W (F)



PLCC32 (B)


PLCC32 (K)


TSOP32 (N)
8 x 20 mm

Contents

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1 Summary description

The M27W401 is a low voltage 4 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage and is organised as 524,288 by 8 bits.

The M27W401 operates in the read mode with a supply voltage as low as 2.7V at –40 to 85°C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

The FDIP32W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For application where the content is programmed only one time and erasure is not required, the M27W401 is offered in PDIP32, PLCC32 and TSOP32 (8 x 20 mm) packages.

In order to meet environmental requirements, ST offers the M27W401 in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at: www.st.com.

See *Figure 1: Logic Diagram* and *Table 1: Signal descriptions* for a brief overview of the signals connected to this device.

Figure 1. Logic Diagram

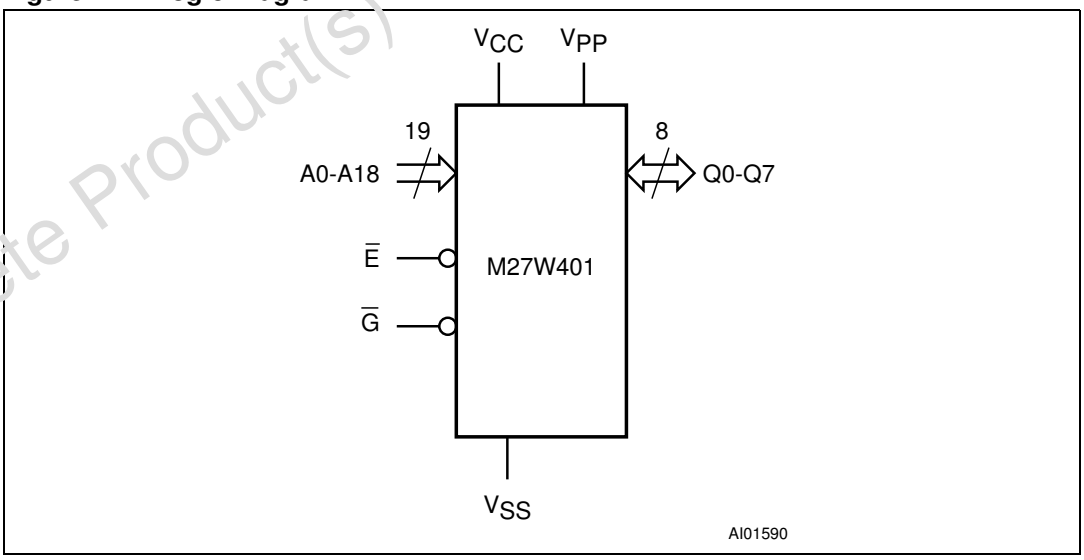


Table 1. Signal descriptions

Signal	Description
A0-A18	Address Inputs
Q0-Q7	Data Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{PP}	Program Supply
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2. DIP Connections

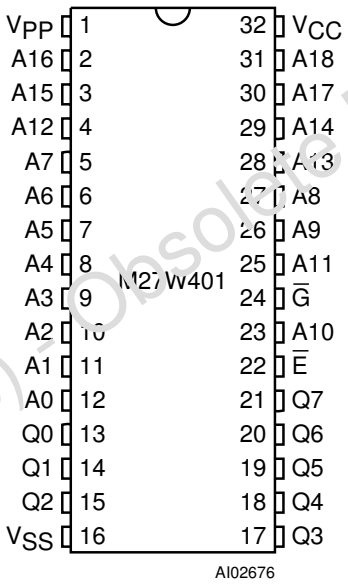


Figure 3. LCC Connections

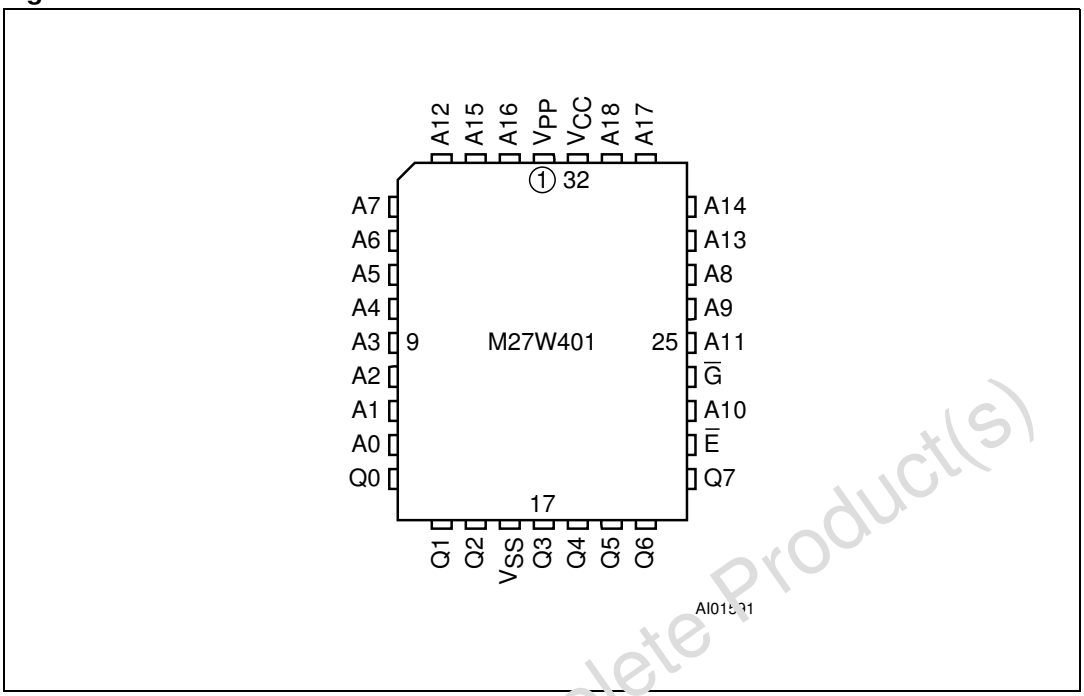
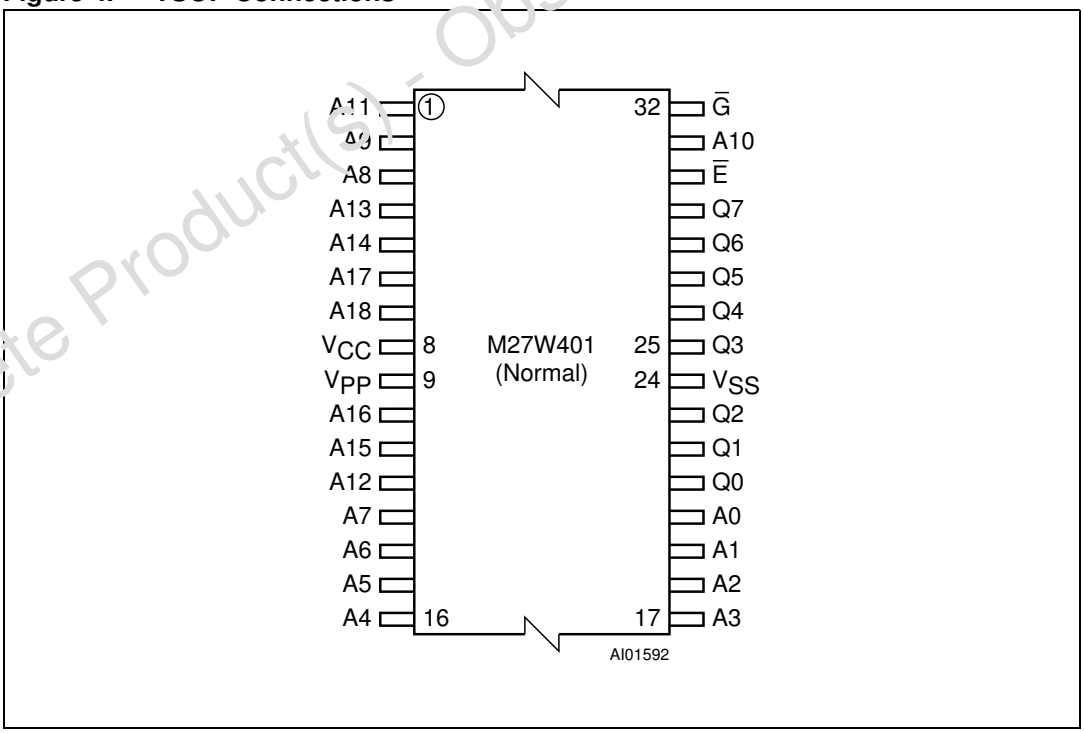


Figure 4. TSOP Connections



2 Device description

Table 2 lists the operating modes of the M27W40. A single power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A9 for Electronic Signature.

Table 2. Operating modes

Mode	$\overline{E}$	$\overline{G}$	A9	V_{PP}	Q7-Q0
Read	V_{IL}	V_{IL}	X	V_{CC} or V_{SS}	Data Out
Output Disable	V_{IL}	V_{IH}	X	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL} Pulse	V_{IH}	X	V_{PP}	Data In
Verify	V_{IH}	V_{IL}	X	V_{PP}	Data Out
Program Inhibit	V_{IH}	V_{IH}	X	V_{PP}	Hi-Z
Standby	V_{IH}	X	X	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	V_{CC}	Codes

Note: X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

2.1 Read mode

The M27W401 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from E to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

2.2 Standby mode

The M27W401 has a standby mode which reduces the supply current from 15mA to 15µA with low voltage operation $V_{CC} \leq 3.6V$, see Read Mode DC Characteristics table for details. The M27W401 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}$ input.

2.3 Two-line output control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all

devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

2.4 System considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

2.5 Programming

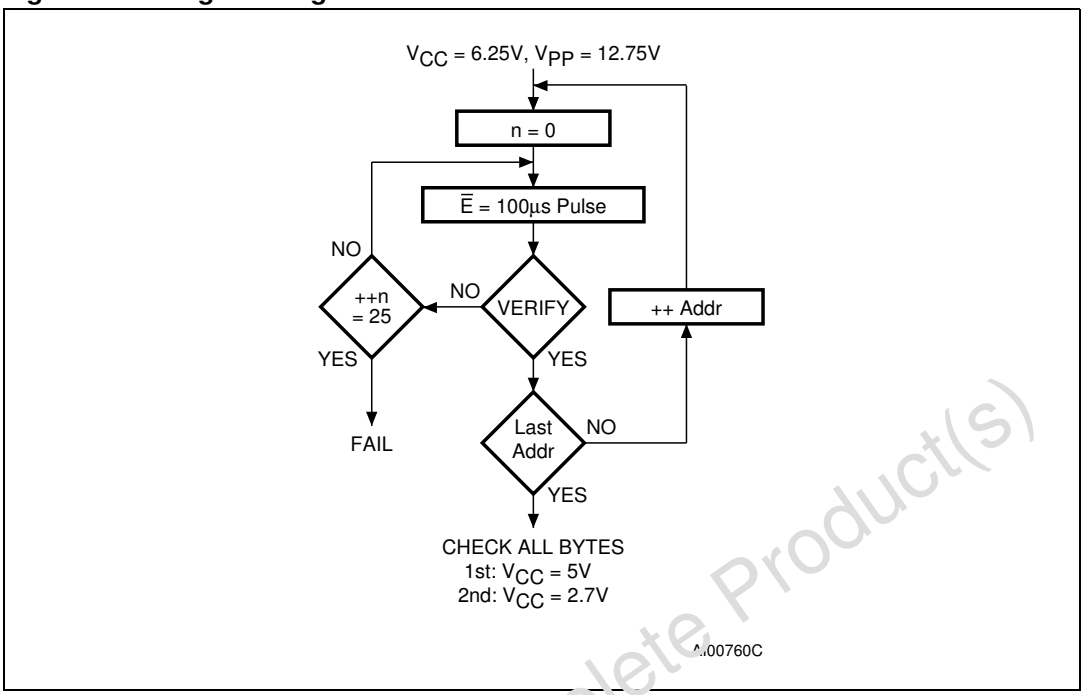
The M27W401 has been designed to be fully compatible with the M27C4001 and has the same electronic signature. As a result the M27W401 can be programmed as the M27C4001 on the same programming equipment applying 12.75V on V_{PP} and 6.25V on V_{CC} by the use of the same PRESTO II algorithm.

When delivered (and after each ‘1’s erasure for UV EPROM), all bits of the M27W401 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a ‘0’ to a ‘1’ is by die exposure to ultraviolet light (UV EPROM). The M27W401 is in the programming mode when V_{PP} input is at 12.75V, $\overline{G}$ is at V_{IH} and $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V

2.6 Presto II programming algorithm

Presto II Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. Programming with Presto II consists of applying a sequence of 100µs program pulses to each byte until a correct verify occurs (see *Figure 5*). During programming and verify operation, a Margin mode circuit is automatically activated in order to guarantee that each cell is programmed with enough margin. No overprogram pulse is applied since the verify in Margin mode at VCC much higher than 3.6V, provides the necessary margin to each programmed cell.

Figure 5. Programming flowchart



2.7 Program Inhibit

Programming of multiple M27W401s in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}$ of the parallel M27W401 may be common. A TTL low level pulse applied to a M27W401's $\overline{E}$ input, with V_{PP} at 12.75V, will program that M27W401. A high level $\overline{E}$ input inhibits the other M27W401s from being programmed.

2.8 Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}, $\overline{E}$ at V_{IH}, V_{PP} at 12.75V and V_{CC} at 6.25V.

2.9 Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27W401. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27W401 with $V_{PP} = V_{CC} = 5V$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the STMicroelectronics

M27W401, these two identifier bytes are given in *Table 3* and can be read-out on outputs Q7 to Q0. Note that the M27W401 and M27C4001 have the same identifier bytes.

Table 3. Electronic Signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device Code	V_{IH}	0	1	0	0	0	0	0	1	41h

2.10 Erasure operation (applies to UV EPROM)

The erasure characteristics of the M27W401 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M27W401 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27W401 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27W401 window to prevent unintentional erasure. The recommended erasure procedure for the M27W401 is exposure to short wave ultraviolet light which has wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 µW/cm^2 power rating. The M27W401 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

3 Maximum ratings

Table 4. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (2)	–40 to 85	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (3)	Input or Output Voltage (except A9)	–2 to 7	V
V_{CC}	Supply Voltage	–2 to 7	V
V_{A9} (3)	A9 Voltage	–2 to 13.5	V
V_{PP}	Program Supply Voltage	–2 to 14	V

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Depends on range.
3. Minimum DC voltage on Input or Output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is VCC +0.5V with possible overshoot to VCC +2V for a period less than 20ns.

4 DC and AC parameters

T_A = –40 to 85°C; V_{CC} = 2.7V to 3.6V; V_{PP} = V_{CC}

Table 5. Read Mode DC Characteristics (1)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC}	Supply Current	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, I_{OUT} = 0mA, f = 5MHz, $V_{CC} \le 3.6V$		15	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V$, $V_{CC} \le 3.6V$		15	µA
I_{PP}	Program Current	$V_{PP} = V_{CC}$		100	µA
V_{IL}	Input Low Voltage		–0.6	$0.2V_{CC}$	V
V_{IH} (2)	Input High Voltage		$0.7V_{CC}$	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400µA	2.4		V

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V

Table 6. Programming Mode DC Characteristics (1)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±10	µA
I_{CC}	Supply Current			50	mA
I_{PP}	Program Current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage TTL	I_{OH} = –400 µA	2.4		V
V_{ID}	A9 Voltage		11.5	12.5	V

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 7. AC Measurement Conditions

Parameter	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

T_A = 25 °C, f = 1 MHz

Table 8. Capacitance (1)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

1. Sampled only, not 100% tested.

Figure 6. AC Testing Input Output Waveform

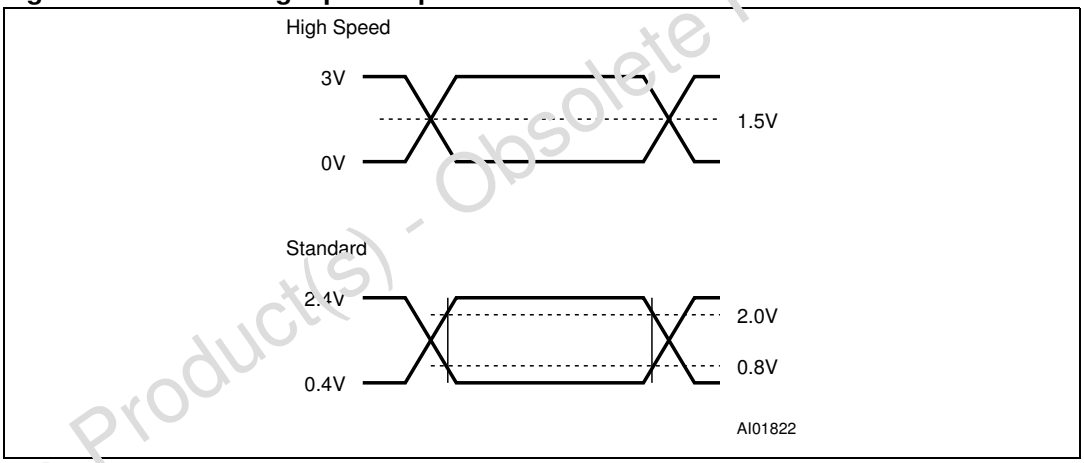
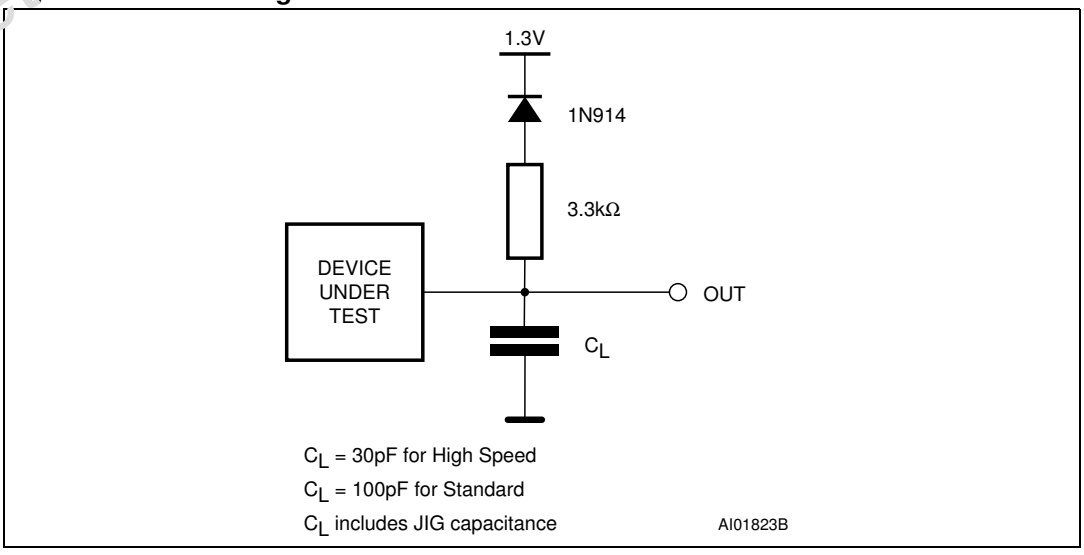


Figure 7. AC Testing Load Circuit



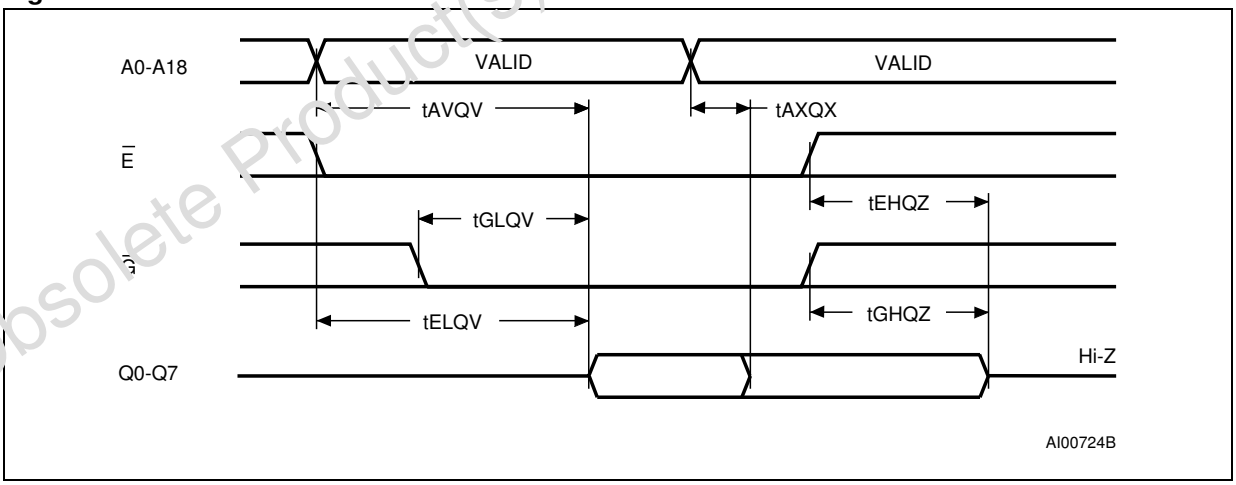
T_A = –40 to 85 °C; V_{CC} = 2.7V to 3.6V; V_{PP} = V_{CC}

Table 9. Read Mode AC Characteristics (1)

Symbol	Alt	Parameter	Test Condition	-80 (2)				-100 (-120/-150/-200)		Unit
				V_{CC} = 3.0V to 3.6V		V_{CC} = 2.7V to 3.6V		V_{CC} = 2.7V to 3.6V		
				Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		100	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		80		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		40		50		60	ns
t_{EHQZ} (3)	t_{DF}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}	0	50	0	50	0	60	ns
t_{GHQZ} (3)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}	0	50	0	50	0	60	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Speed obtained with High Speed AC measurement conditions.
3. Sampled only, not 100% tested.

Figure 8. Read Mode AC Waveforms



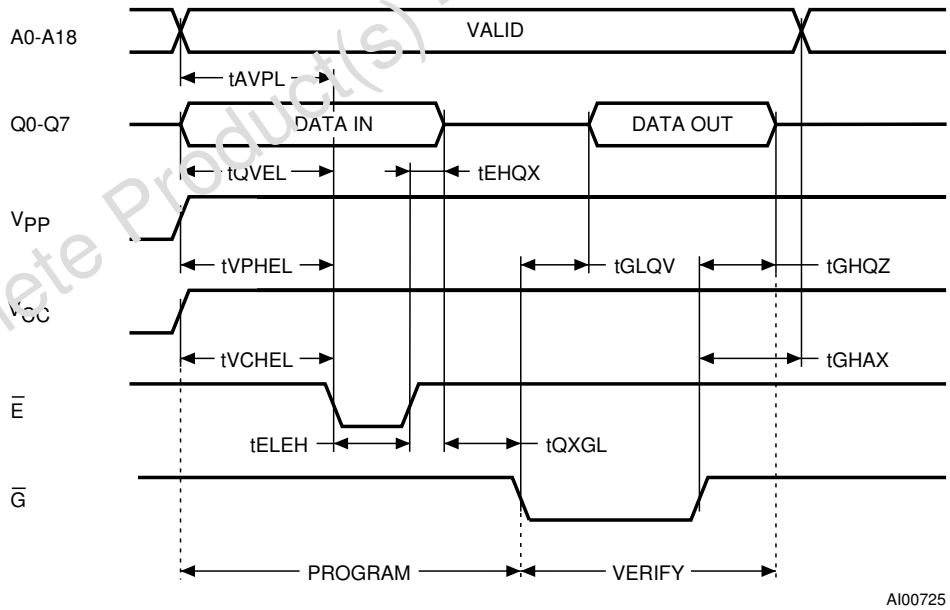
T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V

Table 10. Programming Mode AC Characteristics (1)

Symbol	Alt	Parameter	Test Condition	Min.	Max.	Unit
t_{AVPL}	t_{AS}	Address Valid to Program Low		2		µs
t_{QVPL}	t_{DS}	Input Valid to Program Low		2		µs
t_{VPHPL}	t_{VPS}	V_{PP} High to Program Low		2		µs
t_{VCHPL}	t_{VCS}	V_{CC} High to Program Low		2		µs
t_{ELPL}	t_{CES}	Chip Enable Low to Program Low		2		µs
t_{PLPH}	t_{PW}	Program Pulse Width		95	105	µs
t_{PHQX}	t_{DH}	Program High to Input Transition		2		µs
t_{QXGL}	t_{OES}	Input Transition to Output Enable Low		2		µs
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid			100	ns
t_{GHQZ} (2)	t_{DFP}	Output Enable High to Output Hi-Z		0	130	ns
t_{GHAX}	t_{AH}	Output Enable High to Address Transition		0		ns

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Sampled only, not 100% tested.

Figure 9. Programming and Verify Modes AC Waveforms



5 Package mechanical data

5.1 32-pin Ceramic Frit-seal DIP, with round window (FDIP32WA)

Figure 10. FDIP32WA package outline

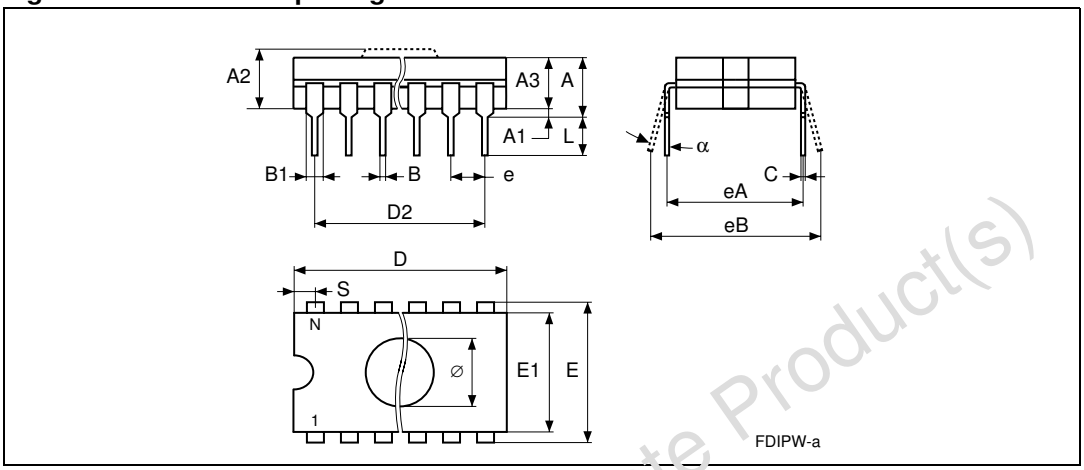


Table 11. FDIP32WA package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.72			0.225
A1	0.51		1.40	0.020		0.055
A2	3.91		4.57	0.154		0.180
A3	3.89		4.50	0.153		0.177
B	0.41		0.56	0.016		0.022
B1		1.45			0.057	
C	0.23		0.30	0.009		0.012
D	41.73		42.04	1.643		1.655
D2		38.10			1.500	
e		2.54			0.100	
E		15.24			0.600	
E1	13.06		13.36	0.514		0.526
eA		14.99			0.590	
eB	16.18		18.03	0.637		0.710
L	3.18		4.10	0.125		0.161
N		32			32	
S	1.52		2.49	0.060		0.098
Ø		7.11			0.280	
α	4°		11°	4°		11°

5.2 32-pin Plastic DIP, 600 mils width (PDIP32)

Figure 11. PDIP32 package outline

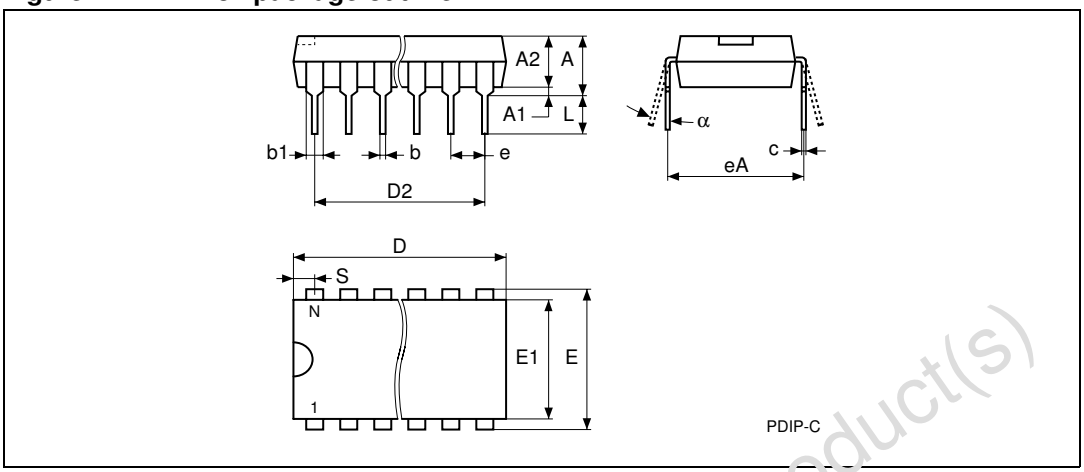


Table 12. PDIP32 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.080			0.2000
A1	0.381			0.0150		
A2		3.912			0.1540	
b	0.406		0.559	0.0160		0.0220
b1	1.168		1.372	0.0460		0.0540
c	0.203		0.356	0.0080		0.0140
D	41.402		42.418	1.6300		1.6700
D2		38.100			1.5000	
E	15.240			0.6000		
E1	13.890		14.248	0.5469		0.5609
e	–	2.540	–	–	0.1000	–
eA	–	15.240	–	–	0.6000	–
L	3.175		3.429	0.1250		0.1350
N		32			32	
S	1.650		2.210	0.0650		0.0870
α	0°		15°	0°		15°

5.3 32-lead Rectangular Plastic Leaded Chip Carrier (PLCC32)

Figure 12. PLCC32 package outline

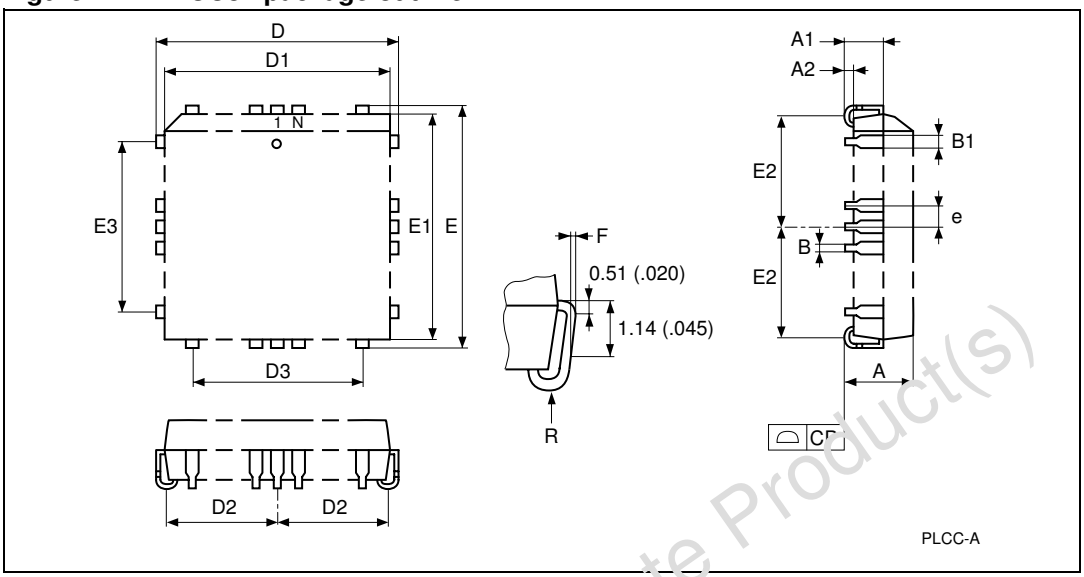


Table 13. PLCC32 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	3.18		3.56	0.125		0.140
A1	1.53		2.41	0.060		0.095
A2	0.38		–	0.015		–
B	0.33		0.53	0.013		0.021
B1	0.66		0.81	0.026		0.032
CP			0.10			0.004
D	12.32		12.57	0.485		0.495
D1	11.35		11.51	0.447		0.453
D2	4.78		5.66	0.188		0.223
D3	–	7.62	–	–	0.300	–
E	14.86		15.11	0.585		0.595
E1	13.89		14.05	0.547		0.553
E2	6.05		6.93	0.238		0.273
E3	–	10.16	–	–	0.400	–
e	–	1.27	–	–	0.050	–
F	0.00		0.13	0.000		0.005
R	–	0.89	–	–	0.035	–
N		32			32	

5.4 32-lead Plastic Thin Small Outline, 8x20 mm (TSOP32)

Figure 13. TSOP32 package outline

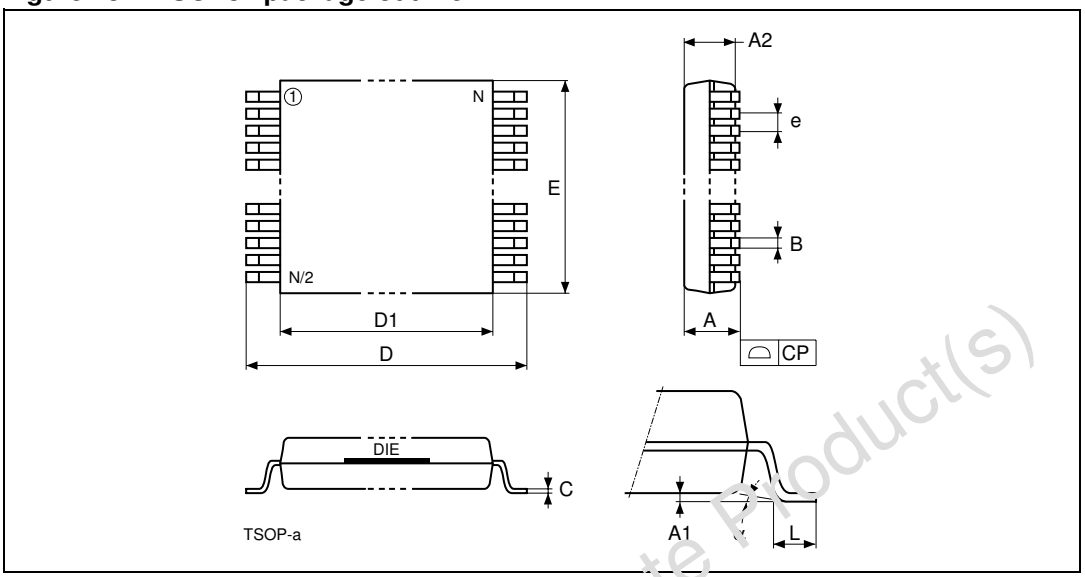
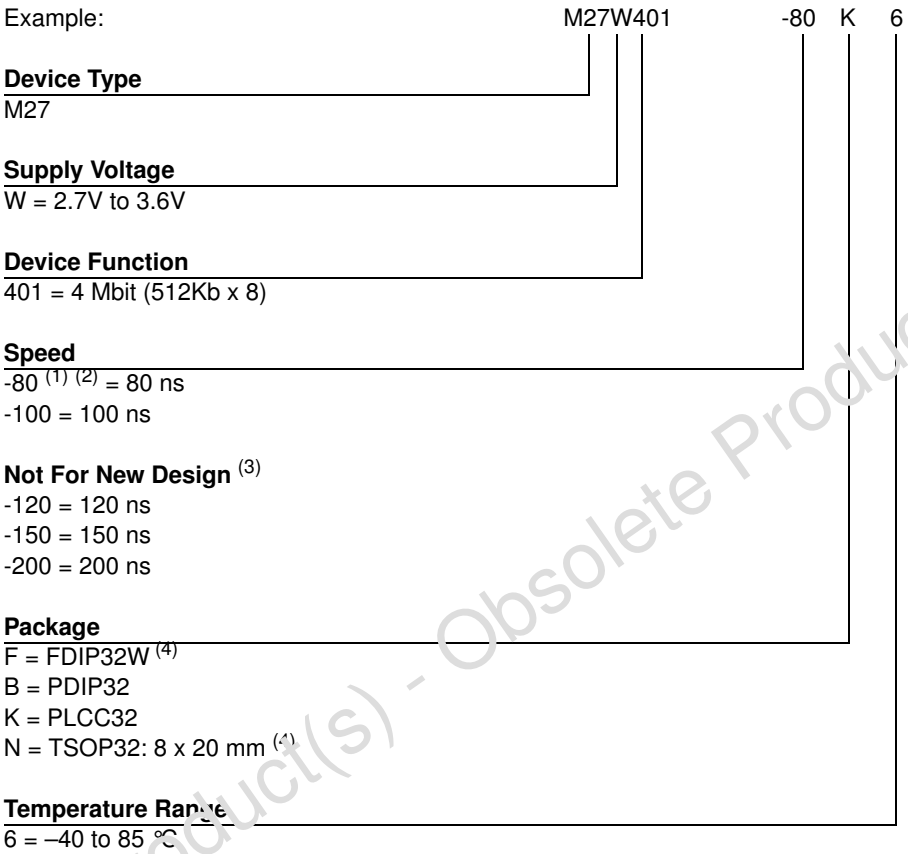


Table 14. TSOP32 package mechanical data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.200			0.0472
A1	0.050		0.150	0.0020		0.0059
A2	0.950		1.050	0.0374		0.0413
B	0.170		0.250	0.0067		0.0098
C	0.100		0.210	0.0039		0.0083
CP			0.100			0.0039
D	19.800		20.200	0.7795		0.7953
D1	18.300		18.500	0.7205		0.7283
e	–	0.500	–	–	0.0197	–
E	7.900		8.100	0.3110		0.3189
L	0.500		0.700	0.0197		0.0276
N		32			32	
α	0°		5°	0°		5°

6 Part numbering

Table 15. Ordering Information Scheme



1. High Speed, see AC Characteristics section for further information.
2. This speed also guarantees 70ns access time at V_{CC} = 3.0V to 3.6V.
3. These speeds are replaced by the 100 ns.
4. Packages option available on request. Please contact STMicroelectronics local Sales Office.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

7 Revision history

Table 16. Document revision history

Date	Revision	Changes
25-Jul-1999	1	First Issue
10-Mar-2000	2	FDIP32W Package Dimension, L Max added (*Table 11*) TSOP32 Package Dimension changed (*Table 14*) 0 to 70°C Temperature Range deleted
21-Apr-2006	3	Converted to new template. Added ECOPACK® information.

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